EXHIBIT A1

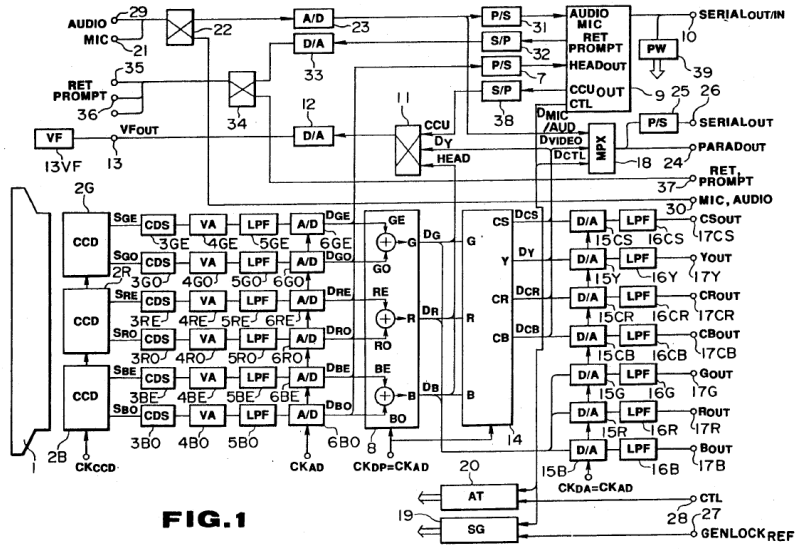
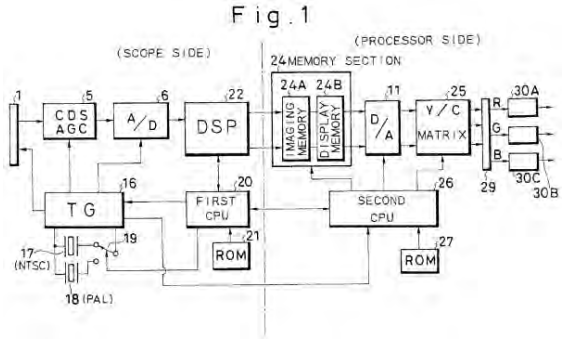
EXHIBIT A1 – INVALIDITY CLAIM CHART FOR U.S. PATENT 7,471,310

U.S. Patent No. 5,166,782 ("Asaida 782")

The asserted claims of the '310 patent are either anticipated by and/or would have been obvious to a person of ordinary skill in the art in view of Asaida 782 either alone or in combination with or further in view of one or more additional references, as described below. Stryker presents the state of the art at the time of the alleged invention of the '310 patent in Section II.B.1, its general obviousness contentions in Section II.B.3, and a technology background in Section II.A, of Stryker's Invalidity Contentions. Stryker incorporates those sections by reference in their entirety.

This chart contains exemplary quotes and citations from prior art references and is not an exhaustive list of every place in the prior art where a claim element may be found. Stryker contends that any claim element not expressly found in the prior art references described below were well known in the art and/or would have been known to a person of ordinary skill in the art at the time of the alleged invention of the '310 patent.

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
1. A video imaging system comprising:	To the extent the preamble is limiting, Asaida 782 discloses "[a] video imaging system." "This invention relates to a video camera forming digital signals representing an object projected on an imaging device and, more particularly, to a video camera having a signal processing circuit for performing digital signal processing on output signals of the imaging device." (Asaida 782 at 1:7-12.) "FIG. 1 is a block diagram showing an embodiment of a camera head unit of a video camera according to the present invention." (Asaida 782 at 3:44-46.)	To the extent the preamble is limiting, Okada 852 discloses "[a] video imaging system." "The present invention relates to an imaging device for an endoscope, and more particularly, it relates to the composition of an endoscope system which can display a picture imaged by using one scope, by either system selected from the NTSC system and the PAL system." (Okada 852 at 1:12-16." "FIG. 1 is a block diagram showing the circuit configuration of an electronic endoscope equipped with both the NTSC system and the PAL system according to an embodiment of the present invention." (Okada 852 at 3:58-61.)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
	 FIG.1 Asaida 782 (Figure 1) "FIG. 3 is a block diagram showing an embodiment of a camera control unit of the video camera shown in FIG. 1." (Asaida 782 at 3:50-52.)	 Okada 852 (Figure 1) To the extent the preamble is limiting, Endsley 613 discloses a video imaging system. Specifically, "[a] block diagram of a multi-mode digital camera with computer interface according to the invention is shown in FIG. 1. The camera 10 is connected to a host computer 12 via a USB (universal serial bus) digital host interface 14, which also provides power to the camera 10. . . . The camera 10 can acquire both still and motion images." (Endsley 613 at 3:7-17.)

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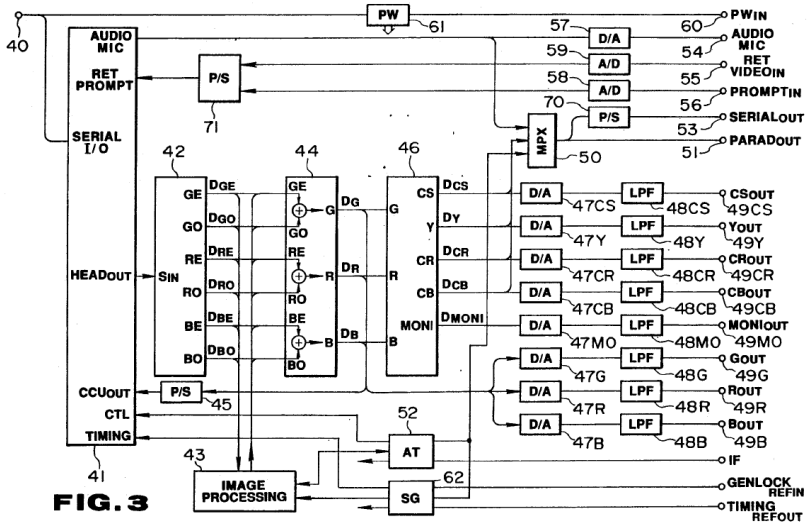
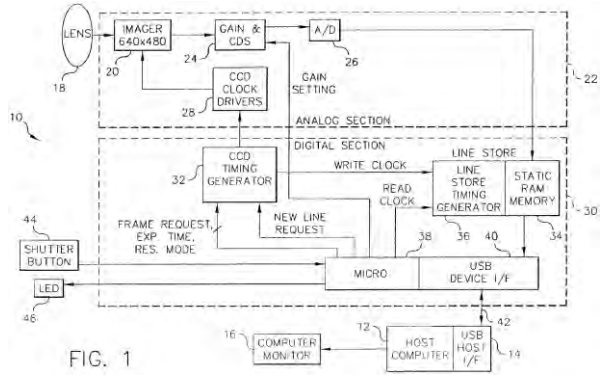
Claims	**Asaida 782**	**in combination with one or more of the following references**
	 FIG. 3 Asaida 782 (Figure 3)	 FIG. 1 Endsley 613 (Figure 1) To the extent the preamble is limiting, Endsley 471 discloses a video imaging system. Specifically, "[a] block diagram of a digital imaging system according to the invention is shown in FIG. 1. The system includes a camera 10 connected to a host computer 12 via a USB (universal serial bus) cable 42 connected to a USB digital host interface 14, which also provides power to the camera 10. . . . The camera 10 can acquire both still and motion images." (Endsley 471 at 2:49-59.)

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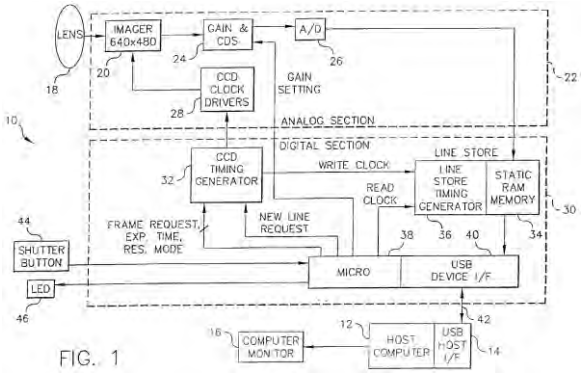
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 FIG. 1 Endsley 471 (Figure 1) To the extent the preamble is limiting, Dowdy 082 discloses "[a] video imaging system." "The invention relates to camera heads for use with remote video display systems such as video endoscopy systems, borescopes, and other devices." (Dowdy 082 at 1:10-12.) "Referring to FIG. 1, a video endoscopy or borescope system 10 includes a camera head 12 and a camera processor 14. Camera head 12 includes an endoscope 16 for insertion into a region such as a body cavity, and an imaging device, such as a CCD 18, that produces electrical signals representative of an optical image at the distal end of endoscope 16. Camera processor 14 processes the electrical signals produced by camera head 12 to generate a video image that is displayed on a video monitor 20." (Dowdy 082 at 3:24-

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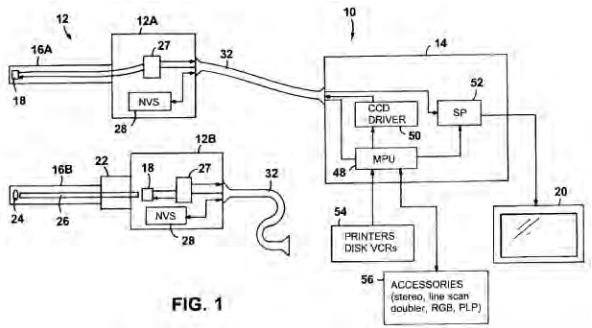
Claims	**Asaida 782**	**in combination with one or more of the following references**
		32.)  FIG. 1 Dowdy 082 (Figure 1) To the extent the preamble is limiting, Oshima 212 discloses "[a] video imaging system. "An endoscope system 1 in accordance with the first embodiment of the present invention shown in FIG. 1 consists broadly of an endoscope 2, and connected apparatuses (or peripheral equipment) to be selectively connected to the endoscope. The connected apparatuses include an image processing apparatus 3A, an image processing apparatus 3B, a cleaning apparatus 3C, a filing apparatus 3D, a monitor 4 a, an image recording apparatus 5 a, a filing apparatus 6 a, a monitor 4 b, an image recording apparatus 5 b, a filing apparatus 6 b, a filing apparatus 6 c, and a monitor 4 d. The image processing apparatus 3A has the ability to communicate with the endoscope 2. . . ." (Oshima 212 at 5:15-26.)

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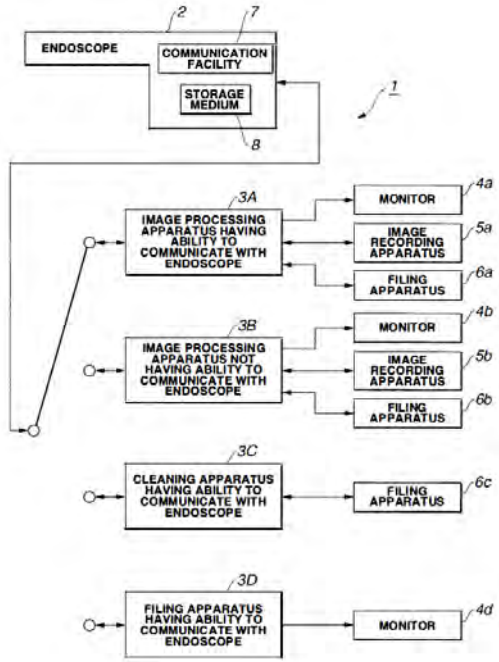
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Oshima 212 (Figure 1) "FIG. 2 is a block diagram showing in detail the endoscope 2 and the image processing apparatus 3A having the communicating ability which are employed in the present embodiment." (Oshima 212 at 6:34-37.)

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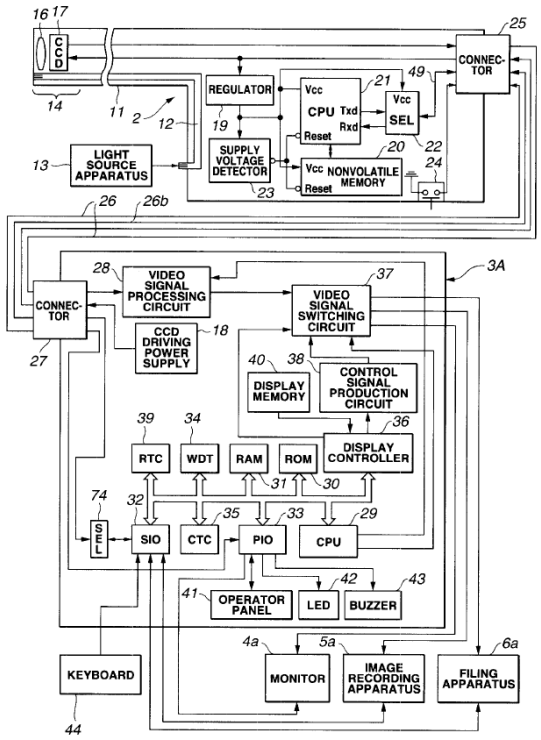
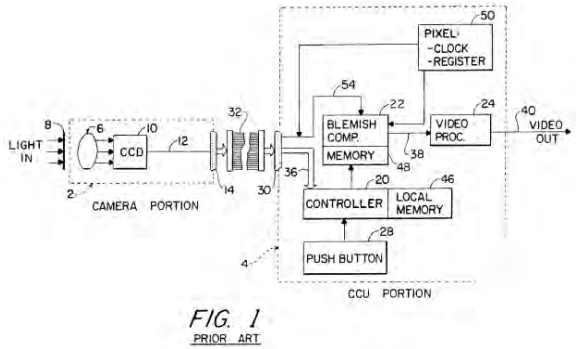
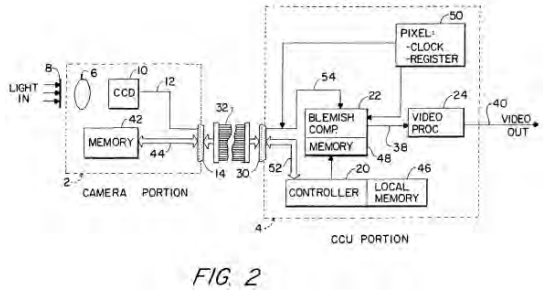
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Oshima 212 (Figure 2) To the extent the preamble is limiting, Zu 391 discloses "[a] video imaging system." "This invention relates to compensating for CCD blemishes in video cameras and ore particularly to cameras that are designed to be used interchangeably with camera control

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		units, notably but not exclusively video cameras that are incorporated in endoscopes for use with medical imaging systems." (Zu 391 at 1.) "Fig. 2 illustrates the invention. Except as described hereinafter, the system shown in Fig. 2 incorporates the same elements and the same functions as the system of Fig. 1, and identical elements are identified by the same numerals." (Zu 391 at 7.)  FIG. 1 PRIOR ART Zu 391 (Figure 1)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 FIG. 2 Zu 391 (Figure 2) To the extent the preamble is limiting, Adler 940 discloses "[a] video imaging system." "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope. The skilled person will appreciate that the wire connection 20 may be an optical connection or may instead use RF or a like means of wireless communication. The miniature endoscopic front-end 10 may be designed for connection to any standard PC input (the USB input for example)." (Adler 940 at 9:24-38.)

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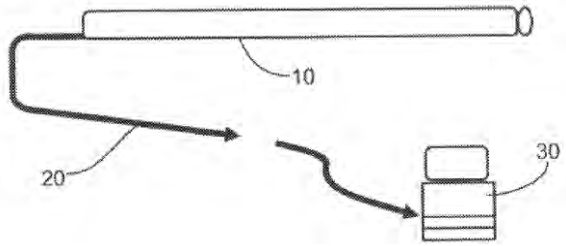
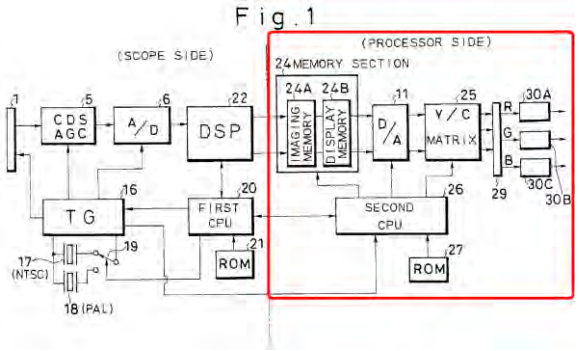
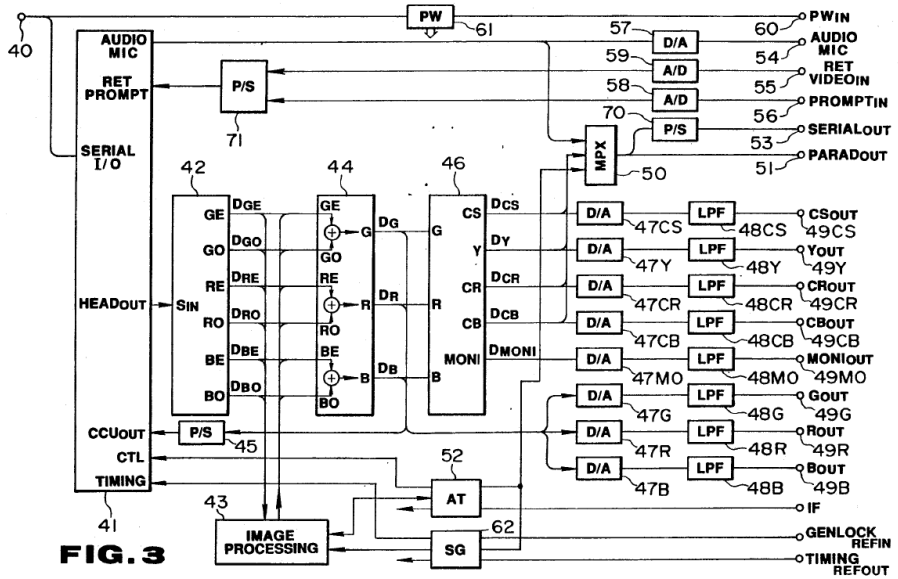
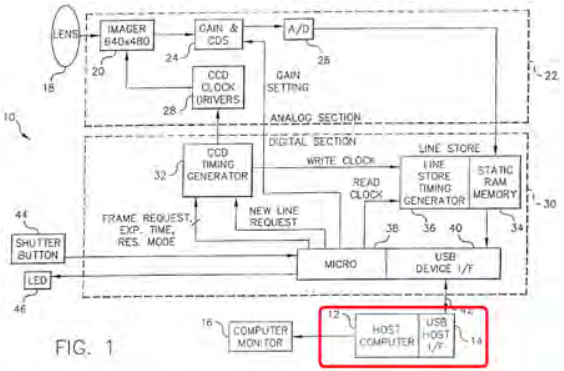
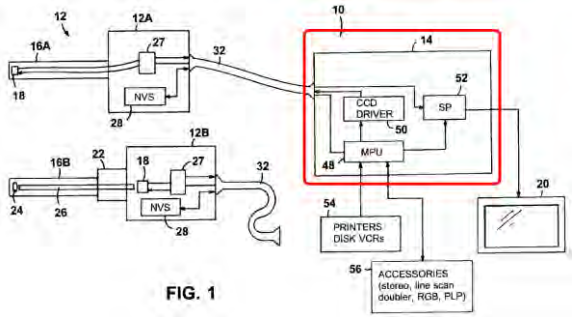
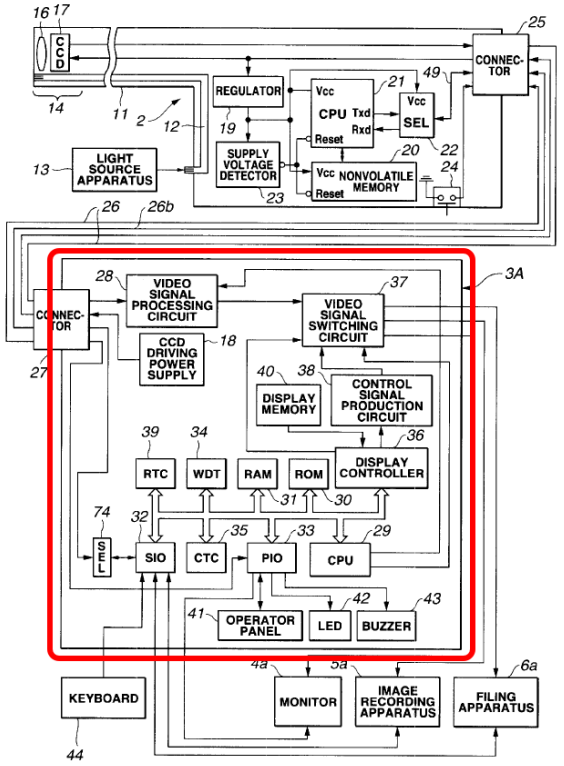
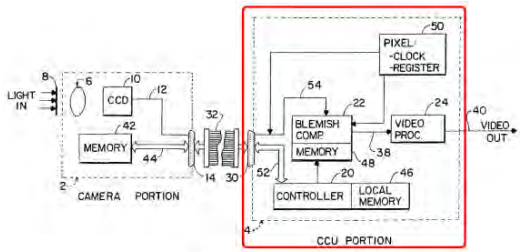
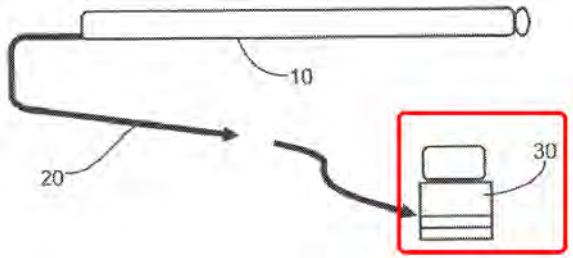
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Adler 940 (Figure 1)
a camera control unit processing a continuous stream of digital video data;	"It is a principal object of the present invention to provide a video camera in which output video signals may be supplied to an external electronic system capable of digital signal processing without the necessity of providing an analog to digital converter at the interface between the video camera and the external electronic system." (Asaida 782 at 1:54-60.) "It is another object of the present invention to provide a video camera which can be electrically connected to an external electronic system capable of digital signal processing by means of a small number of transmission lines." (Asaida 782 at 1:61-65.) "FIG. 3 is a block diagram showing an embodiment of a camera control unit of the video camera shown in FIG. 1." (Asaida 782 at 3:50-52.) "The video camera according to the present invention is constituted by the above mentioned camera head unit shown in FIG. 1 and the	"[O]n the external processor side, a memory section 24 equipped with an imaging memory 24A and a display memory 24B, a D/A converter 11, a brightness/color signal (Y/C) matrix circuit 25, a second CPU 26 for controlling these circuits, and a ROM 27 storing the setting data for the control meeting the selected television system of the NTSC or the PAL are provided." (Okada 852 at 4:34-40.) 

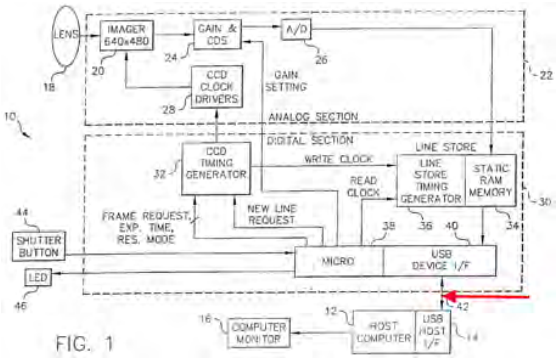
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
	camera control unit CCU arranged and constituted as shown in FIG. 3." (Asaida 782 at 8:1-4.) "The camera control unit CCU, constituting part of the video camera according to the present invention, is provided with a serial input/output port 40, as shown in FIG. 3, which is connected to the serial input/output port 10 of the camera head unit by an optical fiber cable, not shown, constituting transmission means." (Asaida 782 at 8:5-10.)  FIG. 3 Asaida 782 (Figure 3)	Okada 852 (Figure 1) "The system includes a camera 10 connected to a host computer 12 via a USB (universal serial bus) cable 42 connected to a USB digital host interface 14, which also provides power to the camera 10. . . . The camera 10 can acquire both still and motion images. The camera data is processed by the host computer 12 to create final images that can be displayed on a computer monitor 16, e.g., transmitted along with audio as part of a 'computer videoconference', etc." (Endsley 471 at 2:50-63.) "The host computer 12 controls the camera operation. It can instruct the camera 10 when to take still or motion pictures, and set the electronic exposure time via the CCD timing generator 32, and set the analog gain in the CDS/gain block 24 from the microprocessor 38." (Endsley 471 at 3:54-58.)  FIG. 1 Endsley 471 (Figure 1)

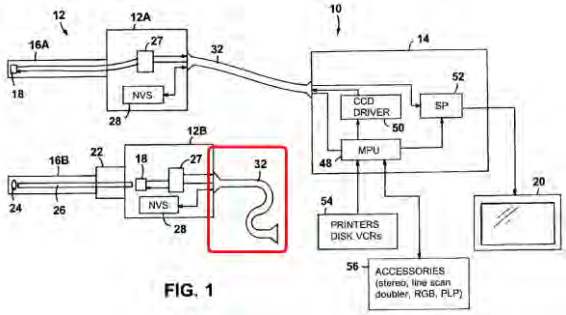
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		"Referring to FIG. 1, a video endoscopy or borescope system 10 includes a camera head 12 and a camera processor 14. Camera head 12 includes an endoscope 16 for insertion into a region such as a body cavity, and an imaging device, such as a CCD 18, that produces electrical signals representative of an optical image at the distal end of endoscope 16. Camera processor 14 processes the electrical signals produced by camera head 12 to generate a video image that is displayed on a video monitor 20." (Dowdy 082 at 3:24-32.)  FIG. 1 Dowdy 082 (Figure 1) "FIG. 2 is a block diagram showing in detail the endoscope 2 and the image processing apparatus 3A having the communicating ability which are employed in the present embodiment." (Oshima 212 at 6:34-37.)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Oshima 212 (Figure 2) "The image processing apparatus 3A consists broadly of a CCD driving power supply 18, a video signal processing circuit 28, a CPU 29, a ROM 30, a RAM 31, a serial controller (S10) 32, a parallel communication controller (PIO) 33, a watchdog timer (WDT) 34, a counter timer (CTC) 35, a display controller 36, a display memory 40, a

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		video signal switching circuit 37, a control signal production circuit 38, a real-time clock (RTC) 39, an operator panel 41, an LED 42, a buzzer 43, and a light adjustment control unit. The CCD driving power supply 18 applies a voltage to the CCD 17 in the endoscope 2. The video signal processing circuit 28 processes a video signal resulting from photoelectric conversion performed by the CCD 17. The CPU 29 carries out a plurality of arithmetic operations." (Oshima 212 at 7:15-27.) "Figure 1 illustrates a prior art video system comprising a camera 2 and a CCU 4. . . . The CCU 4 comprises a controller 20 with local non-volatile digital memory 46, a blemish compensator 22 with associated volatile digital memory 48, a video signal processor 24, a pixel clock/pixel address register 50, a push-button interface and mode selector 28 for directing operation of controller 20." (Zu 391 at 3.)  FIG. 2 Zu 391 (Figure 2)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		"Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope." (Adler 940 at 9:24-33.) "The software included with processing device 30 processes the output of the miniature endoscopic front-end 10. The software may typically control transfer of the images to the monitor of the PC 30 and their display thereon including steps of 3D modeling based on stereoscopic information as will be described below, and may control internal features of the endoscopic front end 10 including light intensity, and automatic gain control (AGC), again as will be described below." (Adler 940 at 9:39-47.)  Adler 940 (Figure 1)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
a cable, connected to said camera control unit, for transmitting the stream of digital video data to said camera control unit; and	"The camera control unit CCU, constituting part of the video camera according to the present invention, is provided with a serial input/output port 40, as shown in FIG. 3, which is connected to the serial input/output port 10 of the camera head unit by an optical fiber cable, not shown, constituting transmission means." (Asaida 782 at 8:5-10 (emphasis added).)	"The system includes a camera 10 connected to a host computer 12 via a USB (universal serial bus) cable 42 connected to a USB digital host interface 14, which also provides power to the camera 10. . . . The camera 10 can acquire both still and motion images. The camera data is processed by the host computer 12 to create final images that can be displayed on a computer monitor 16, e.g., transmitted along with audio as part of a 'computer videoconference', etc." (Endsley 471 at 2:50-63.) "The USB cable 42 includes four wires, one pair for sending data to and from the host computer 12, and a second pair to supply power to the camera 10 from the host." (Endsley 471 at 3:46-48.)  FIG. 1 Endsley 471 (Figure 1) "Referring to FIG. 4, in a more detailed view, camera head 12 includes CCD 18 (located, as discussed, either in the head

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		or at the tip of the endoscope), NVS 28 and a set of button switches 92 for system control, and camera processor 14 includes a camera controller 94 and a signal processor 96. Cable 32, which connects camera head 12 to camera processor 14, carries drive signals from CCD driver 50 in signal processor 96, electrical signals from CCD 18 to a preamplifier 98 in signal processor 96, data between NVS 28 and MPU 48 in camera controller 94, and signals from button switches 92 to MPU 48." (Dowdy 082 at 6:48-58.)  FIG. 1 Dowdy 082 (Figure 1)

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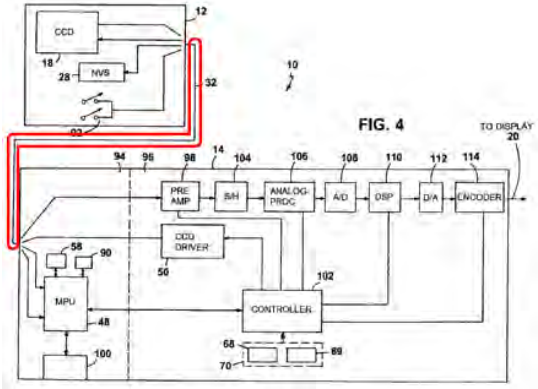
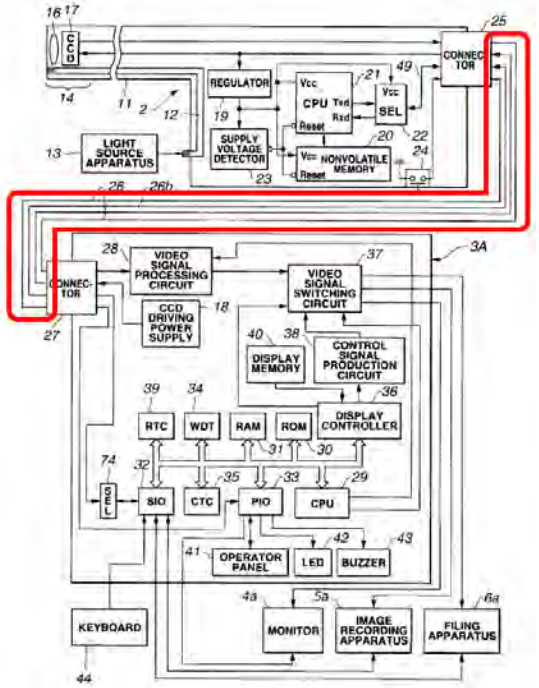
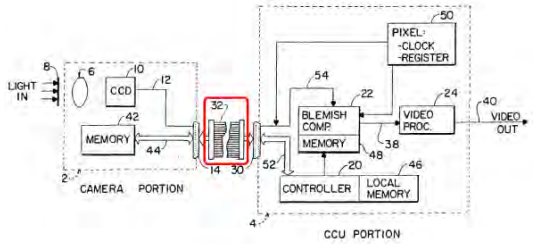
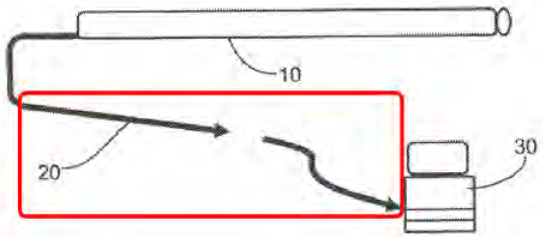
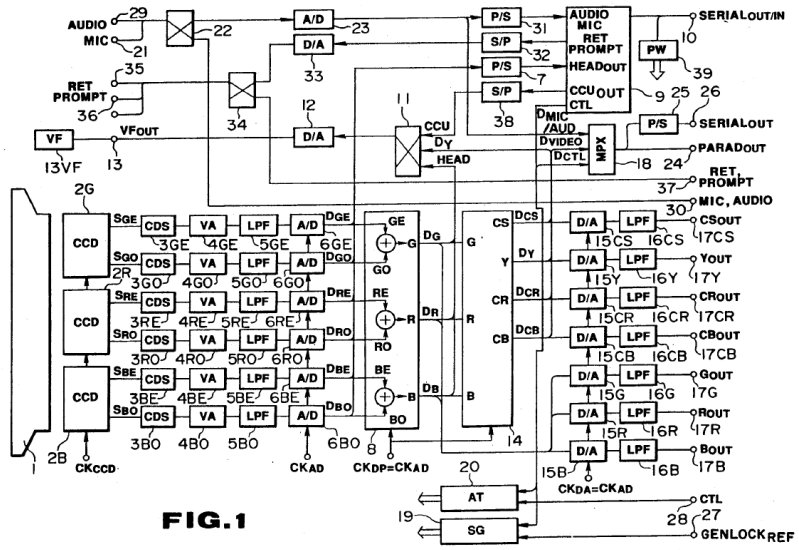
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Dowdy 082 (Figure 4) "The connector 25 of the endoscope 2 is linked to a connector 27 of the image processing apparatus 3A by a cable 26." (Oshima 212 at 7:11-13.)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Oshima 212 (Figure 2) "The CCU 4 also comprises an input connector 30 whereby the CCU may be coupled to camera output connector 14 via a suitable cable 32." (Zu 391 at 3.)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 FIG. 2 Zu 391 (Figure 2) "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope. The skilled person will appreciate that the wire connection 20 may be an optical connection or may instead use RF or a like means of wireless communication. The miniature endoscopic front-end 10 may be designed for connection to any standard PC input (the USB input for example)." (Adler 940 at 9:24-38.)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Adler 940 (Figure 1)
a camera head, connected to said cable, for providing the stream of digital video data, said camera head including;	"FIG. 1 is a block diagram showing an embodiment of a camera head unit of a video camera according to the present invention." (Asaida 782 at 3:44-46.)  FIG.1	"In FIG. 1 and FIG. 2, the circuit configuration of an electronic endoscope according to the embodiment is shown. In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having a number of scanning lines or the like suitable for the scanning line of the NTSC system, and to this CCD 1, a timing generator 16 is connected, and to this timing generator 16, an NTSC crystal oscillator 17, a PAL crystal oscillator 18, and a switching device 19 are provided. Furthermore, a first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU 20, either of the oscillators 17, 18 is selected." (Okada 852 at 4:4-15.)

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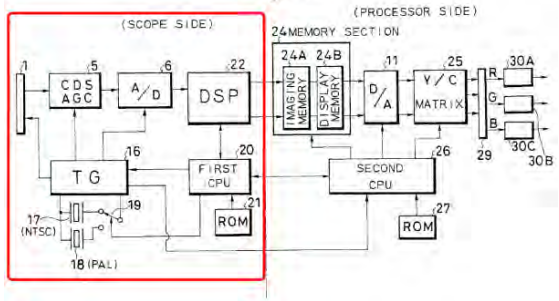
Claims	**Asaida 782**	**in combination with one or more of the following references**
	Asaida 782 (Figure 1) "The encoder/decoder 9 encodes the serial data, that is, the camera output data $HEAD_{OUT}$, supplied from the P/S converter 7, and outputs the encoded data at a serial input/output port 10 over an optical fiber cable, not shown." (Asaida 782 at 5:45-49.) "Thus, with the present video camera unit, the two-line-concurrent three-color imaging output signals S_{RO}, S_{RE}, S_{GO}, S_{GE}, S_{BO} and S_{BE}, obtained by the solid-state image sensors 2R, 2G, and 2B, are changed by the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE into two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}. The two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, are converted by the P/S converter 7 into serial data as the camera output data $HEAD_{OUT}$, which are serially outputted at the serial input/output port 10 by means of the encoder/decoder 9." (Asaida 782 at 5:50-61.)	Fig. 1  Okada 852 (Figure 1) "The system includes a camera 10 connected to a host computer 12 via a USB (universal serial bus) cable 42 connected to a USB digital host interface 14, which also provides power to the camera 10. . . . The camera 10 can acquire both still and motion images. The camera data is processed by the host computer 12 to create final images that can be displayed on a computer monitor 16, e.g., transmitted along with audio as part of a 'computer videoconference', etc." (Endsley 471 at 2:50-63.)

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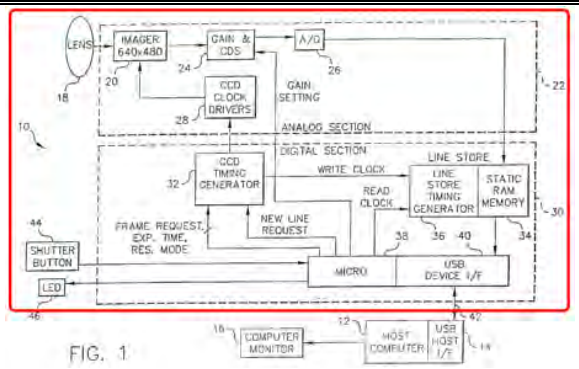
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 FIG. 1 Endsley 471 (Figure 1 "Referring to FIG. 1, a video endoscopy or borescope system 10 includes a camera head 12 and a camera processor 14. Camera head 12 includes an endoscope 16 for insertion into a region such as a body cavity, and an imaging device, such as a CCD 18, that produces electrical signals representative of an optical image at the distal end of endoscope 16. Camera processor 14 processes the electrical signals produced by camera head 12 to generate a video image that is displayed on a video monitor 20." (Dowdy 082 at 3:24-32.) "By varying parameters such as the type of endoscope, the endoscope mount, and the CCD optical format size, camera head 12 can be configured in numerous ways, all of which can produce different electrical signals to represent the same optical image. As illustrated in FIG. 1, camera head 12A includes an electronic endoscope 16A, while camera head

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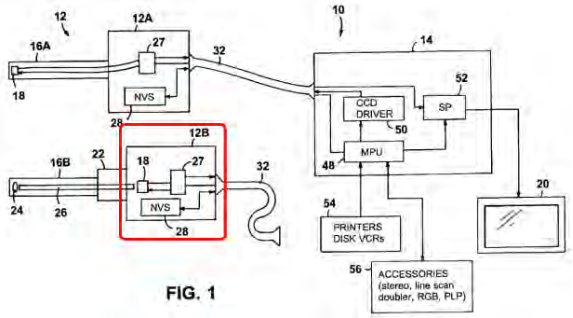
Claims	**Asaida 782**	**in combination with one or more of the following references**
		12B includes an optical endoscope 16B. Electronic endoscope 16A is integrally connected to camera head 12A and has a CCD 18 positioned behind focussing optics (not shown) at its distal end. By contrast, optical endoscope 16B has a mount 22 for attachment to camera head 12B, and includes an optical lens 24 positioned at its distal tip and an optical fiber 26 or relay lens assembly that transmits an image from optical lens 24 to a CCD 18 positioned, with support circuitry 27, within camera head 16B." (Dowdy 082 at 3:33-47 (emphasis added).)  FIG. 1 Dowdy 082 (Figure 1) "Referring to FIG. 4, in a more detailed view, camera head 12 includes CCD 18 (located, as discussed, either in the head or at the tip of the endoscope), NVS 28 and a set of button switches 92 for system control, and camera processor 14 includes a camera controller 94 and a signal processor 96. Cable 32, which connects camera head 12 to camera processor 14, carries drive signals from CCD driver 50 in

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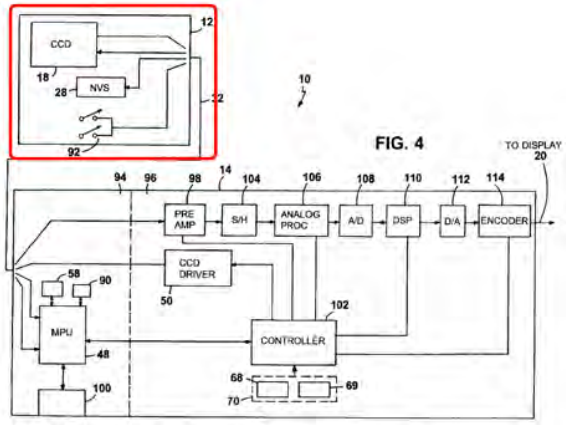
Claims	**Asaida 782**	**in combination with one or more of the following references**
		signal processor 96, electrical signals from CCD 18 to a preamplifier 98 in signal processor 96, data between NVS 28 and MPU 48 in camera controller 94, and signals from button switches 92 to MPU 48." (Dowdy 082 at 6:48-58 (emphasis added).)  Dowdy 082 (Figure 4) "An endoscope system 1 in accordance with the first embodiment of the present invention shown in FIG. 1 consists broadly of an endoscope 2, and connected apparatuses (or peripheral equipment) to be selectively connected to the endoscope. The connected apparatuses include an image processing apparatus 3A, an image processing apparatus 3B, a cleaning apparatus 3C, a filing apparatus 3D, a monitor 4 a, an image recording apparatus 5 a, a filing apparatus 6 a, a monitor 4 b, an image recording

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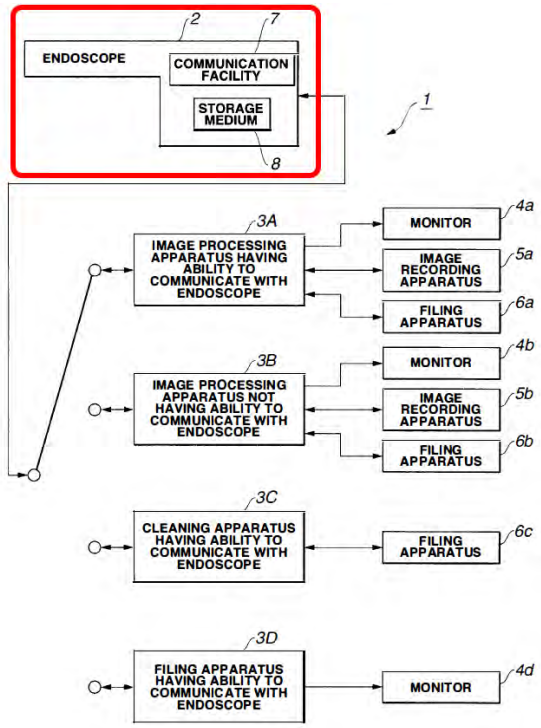
Claims	**Asaida 782**	**in combination with one or more of the following references**
		apparatus 5 b, a filing apparatus 6 b, a filing apparatus 6 c, and a monitor 4 d. The image processing apparatus 3A has the ability to communicate with the endoscope 2. . . ." (Oshima 212 at 5:15-26.)  Oshima 212 (Figure 1) "FIG. 2 is a block diagram showing in detail the endoscope 2 and the image processing apparatus 3A having the

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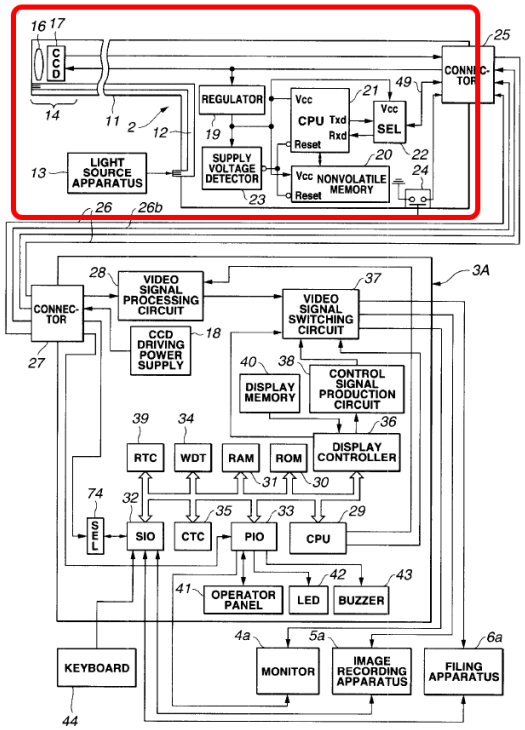
Claims	**Asaida 782**	**in combination with one or more of the following references**
		communicating ability which are employed in the present embodiment." (Oshima 212 at 6:34-37.)  Oshima 212 (Figure 2) "The connector 25 of the endoscope 2 is linked to a connector 27 of the image processing apparatus 3A by a cable 26." (Oshima 212 at 7:11-13.)

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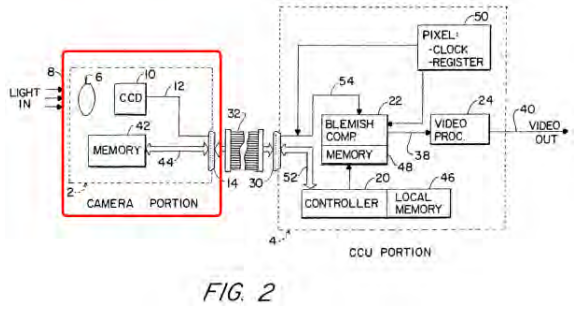
Claims	**Asaida 782**	**in combination with one or more of the following references**
		"Figure 1 illustrates a prior art video system comprising a camera 2 and a CCU 4. The camera comprises an optical system 6 and a CCD array 10. The latter produces a video signal output when it is illuminated with light via optical system 6. This video signal output is fed by an internal transmission bus 12 to an output connector 14 which forms part of the camera." (Zu 391 at 3.)  FIG. 2 Zu 391 (Figure 2) "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope. The skilled person will appreciate

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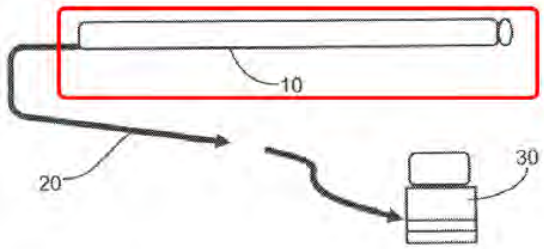
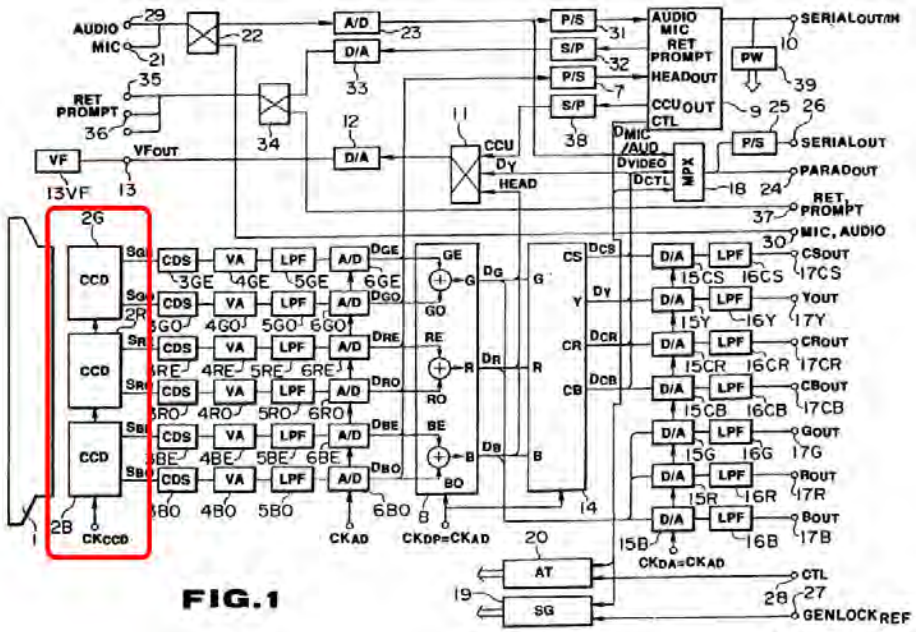
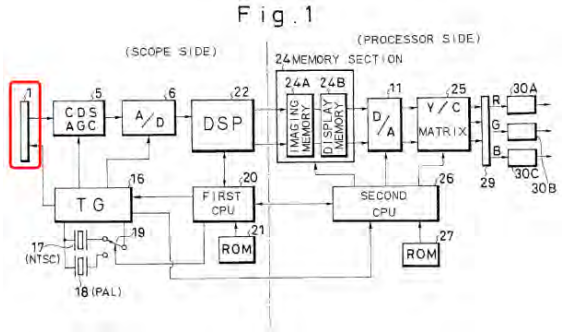
Claims	**Asaida 782**	**in combination with one or more of the following references**
		that the wire connection 20 may be an optical connection or may instead use RF or a like means of wireless communication. The miniature endoscopic front-end 10 may be designed for connection to any standard PC input (the USB input for example)." (Adler 940 at 9:24-38.)  Adler 940 (Figure 1)
an imager, for generating an analog stream of video data;	"In the camera head unit, shown in FIG. 1, the present invention includes a three CCD solid state color imaging device in which the imaging light from an object in a field of view is separated by an imaging pickup device 1 into three primary color components and in which three primary color object images are produced by three solid state imaging sensors 2R, 2G and 2B." (Asaida 782 at 4:9-15.)	"In FIG. 1 and FIG. 2, the circuit configuration of an electronic endoscope according to the embodiment is shown. In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having a number of scanning lines or the like suitable for the scanning line of the NTSC system, and to this CCD 1, a timing generator 16 is connected, and to this timing generator 16, an NTSC crystal oscillator 17, a PAL crystal oscillator 18, and a switching device 19 are provided. Furthermore, a first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU 20, either of the oscillators 17, 18 is selected." (Okada 852 at 4:4-15.)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
	 FIG.1 Asaida 782 (Figure 1)	 Okada 852 (Figure 1) "The camera 10 includes an optical section 18 from imaging light from a subject upon an electronic image sensor 20. A preferred image sensor is a Kodak KAI-0320CM interline transfer, progressive-scan charge-coupled-device (CCD) image sensor with a usable active image area having 640 columns and 480 rows of color photoelements arranged in the well-known Bayer color filter array patters shown in FIG. 2 (see U.S. Pat. No. 3,971,065 for further description of the Bayer pattern). As shown in FIG. 2, the sensor 20 includes light shielded vertical registers 50 and a horizontal readout register 52. Details of a single photoelement 54 are shown in FIG. 3. Each photoelement 54 includes a light-sensitive photodiode 56 supported on a substrate 58 adjacent the light-shielded vertical register 50." (Endsley 471 at 2:66-3:12.) "An analog section 22 in the camera 10 includes the sensor 20, a CDS/gain block 24 for performing correlated double

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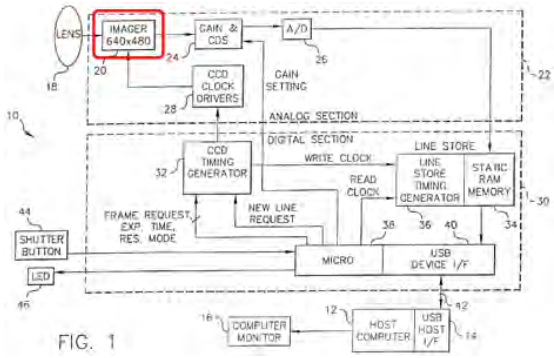
Claims	**Asaida 782**	**in combination with one or more of the following references**
		sampling (CDS) and setting the analog gain, an analog-to-digital (A/D) converter 26 for converting the analog output signal from the CCD sensor 20 to, e.g., an 8-bit digital signal, and CCD clock drivers 28 for clocking the sensor 20." (Endsley 471 at 3:13-18.)  Endsley 471 (Figure 1) "Referring to FIG. 1, a video endoscopy or borescope system 10 includes a camera head 12 and a camera processor 14. Camera head 12 includes an endoscope 16 for insertion into a region such as a body cavity, and an imaging device, such as a CCD 18, that produces electrical signals representative of an optical image at the distal end of endoscope 16. Camera processor 14 processes the electrical signals produced by camera head 12 to generate a video image that is displayed on a video monitor 20." (Dowdy 082 at 3:24-32.)

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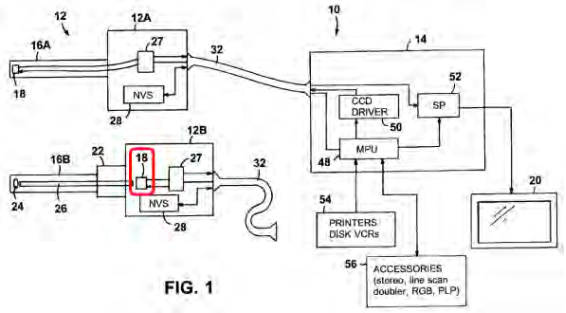
Claims	**Asaida 782**	**in combination with one or more of the following references**
		"By varying parameters such as the type of endoscope, the endoscope mount, and the CCD optical format size, camera head 12 can be configured in numerous ways, all of which can produce different electrical signals to represent the same optical image. As illustrated in FIG. 1, camera head 12A includes an electronic endoscope 16A, while camera head 12B includes an optical endoscope 16B. Electronic endoscope 16A is integrally connected to camera head 12A and has a CCD 18 positioned behind focussing optics (not shown) at its distal end. By contrast, optical endoscope 16B has a mount 22 for attachment to camera head 12B, and includes an optical lens 24 positioned at its distal tip and an optical fiber 26 or relay lens assembly that transmits an image from optical lens 24 to a CCD 18 positioned, with support circuitry 27, within camera head 16B." (Dowdy 082 at 3:33-47 (emphasis added).)  FIG. 1 Dowdy 082 (Figure 1) "The output of preamplifier 98 is connected to the input of a

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		sample and hold circuit 104 that passes only portions of the output. The output of sample and hold circuit 104 is supplied to an analog processing circuit 106 that is also controlled by signal processing controller 102. In controlling analog processing circuit 106, signal processing controller 102 uses values from lookup table 68 that have been loaded into memory 70. As discussed above, if these values have been modified or replaced by MPU 48 based on information from NVS 28 of camera head 12, then analog processing circuit 106 will be affected by the new values." (Dowdy 082 at 7:27-37.) "An analog to digital converter 108 converts the output of analog processing circuit 106 into a digital signal, and supplies the digital signal to a digital signal processor (DSP) 110 that is controlled by signal processing controller 102. Once again, signal processing controller 102 controls digital signal processor using values from memory 70 that can be modified or replaced by MPU 48 in response to information from NVS 28 of camera head 12." (Dowdy 082 at 7:38-45.) Because digital-to-analog conversion takes place in the CCU, the imager 18 must generate an analog stream of video data. "The illuminated object is imaged by a solid-state imaging device located on an image plane, for example, a charge-coupled device (CCD) 17 through an objective 16 locked in an observation window formed in the distal part 14. The CCD 17 photoelectrically converts the optical image." (Oshima 212 at 6:49-53.)

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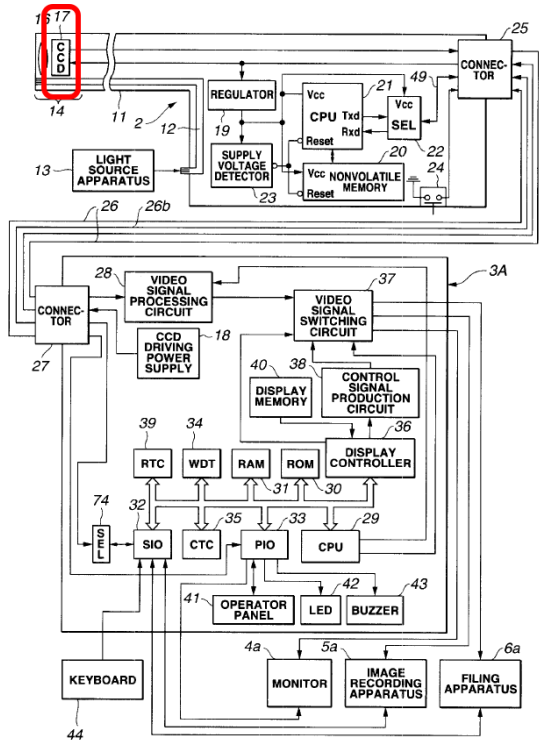
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Oshima 212 (Figure 2) "Figure 1 illustrates a prior art video system comprising a camera 2 and a CCU 4. The camera comprises an optical system 6 and a CCD array 10. The latter produces a video signal output when it is illuminated with light via optical system 6. This video signal output is fed by an internal

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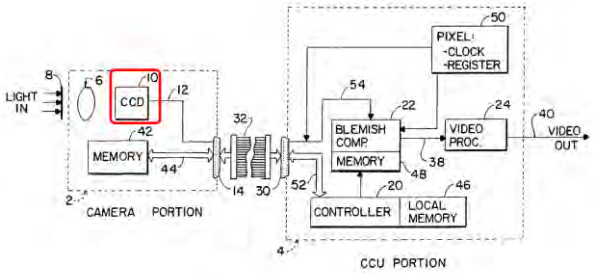
Claims	**Asaida 782**	**in combination with one or more of the following references**
		transmission bus 12 to an output connector 14 which forms part of the camera." (Zu 391 at 3 (emphasis added).)  FIG. 2 Zu 391 (Figure 2) "Reference is now made to FIG. 2, which is an internal block diagram of an endoscope according to a preferred embodiment of the present invention. A miniature endoscope 40 is connected by a wire 42 to an adapter 44. The endoscope 40 comprises an image sensor 46 which may typically comprise a CMOS or CCD or like sensing technology, an optical assembly 48, a light or illumination source 50, communication interface 52 and controller 54. The wired unit of FIG. 2 preferably includes a voltage regulator 56." (Adler 940 at 9:48-57.)

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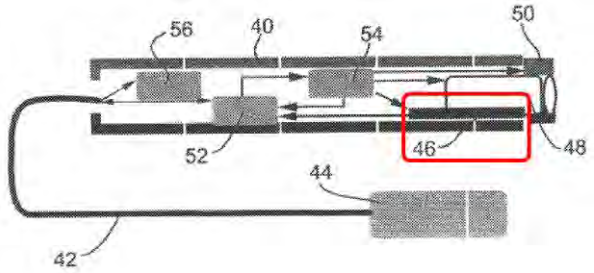
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Adler 940 (Figure 2) "The present invention relates generally to the field of interface circuits, and more particularly, to interface circuitry for providing selectable single-ended and differential signal output from a CMOS image sensor to an external digital signal processor." (Chung 290 at 1:11-15.) "One of the advantages of CMOS image sensors (CMOS imagers) over CCD imagers is that the CMOS imager chip can include digital signal processing circuitry. In practice, the signal processing is more often performed on a companion chip, in order to provide greater application flexibility. However, CMOS imagers often have integrated analog to digital converters to convert the analog signal to a digital bit stream that can be processed by the companion chip. The digitized information then must be transferred to companion chip or other external devices for picture storage, processing, or transmission." (Chung 290 at 1:17-27.) "FIG. 4 illustrates CMOS video imaging sensing circuitry

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		according to the preferred embodiment disclosed in co-pending U.S. application Ser. No 09/062,343. This circuitry includes a CMOS image sensor chip 50 and an image processor chip 52. The CMOS image sensor chip 50 typically includes a number of light responsive CMOS pixel sensors which develop analog signals representative of an image. These analog signals are then A to D converted by the ADC circuit to form digital signals Din0, Din1 . . . Dinn. The image processor chip 52 includes a data processor 53 which performs various manipulations of the image data such as compression and color processing. The processor 53 may be software driven or a hardware embodiment." (Chung 290 at 2:14-26.)

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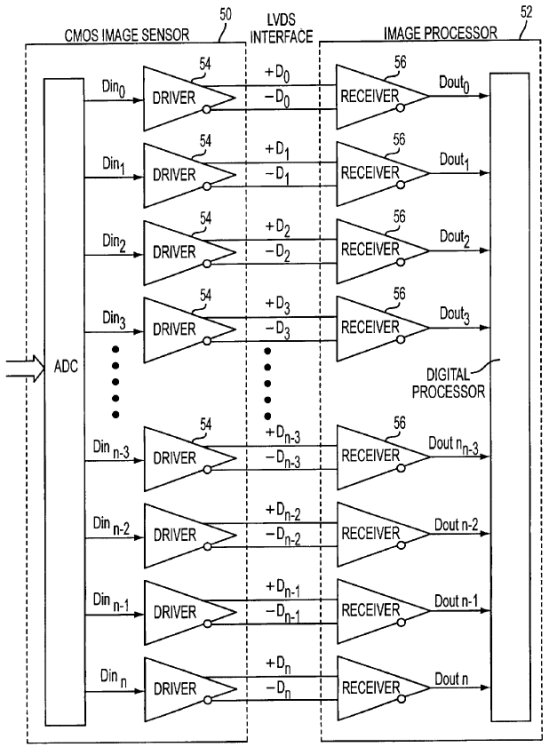
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Chung 290 (Figure 4)
a timing generator, generating a timing signal particular to	"The three solid-state image sensors 2R, 2G and 2B, each formed as an above described two-line-concurrent reading high resolution CCD image sensor 2, are driven by a CCD driving circuit, not shown, using a driving clock CK_{CCD} having a frequency of, for example, 21.5 MHz." (Asaida 782 at 4:41-46.)	"In FIG. 1 and FIG. 2, the circuit configuration of an electronic endoscope according to the embodiment is shown. In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having a number of scanning lines or the like suitable for the scanning line of the NTSC system, and to this CCD 1, a timing generator 16 is

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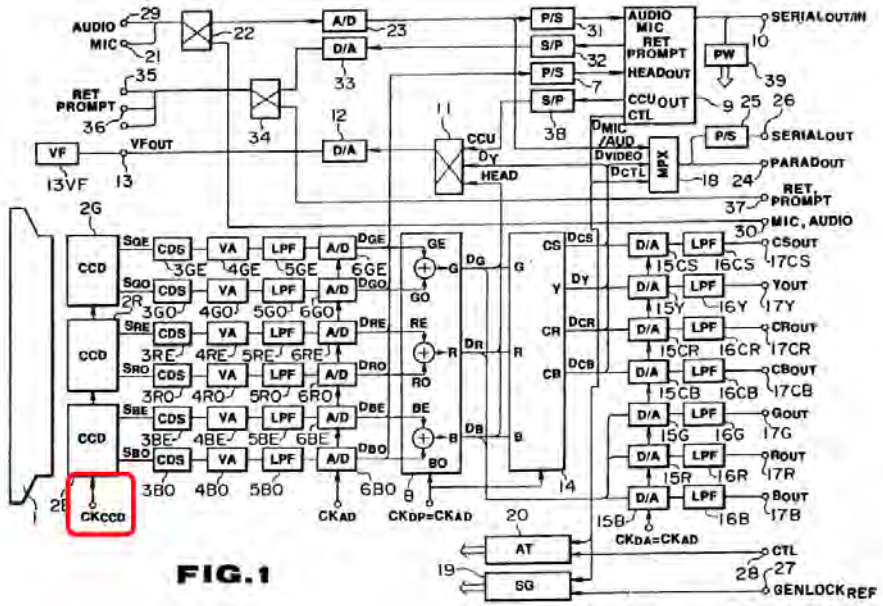
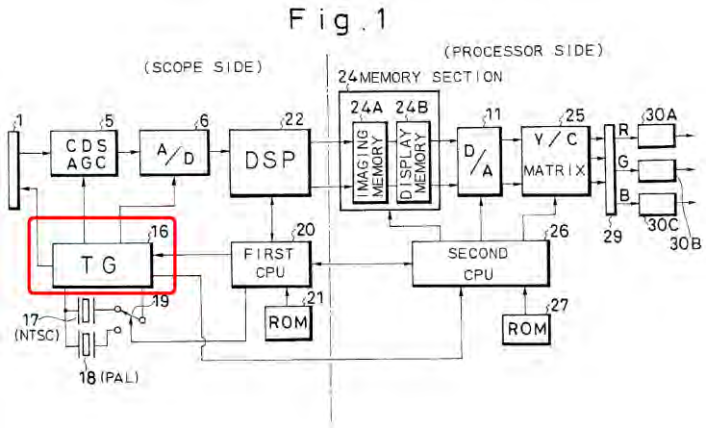
Claims	**Asaida 782**	**in combination with one or more of the following references**
said camera head, the timing signal actuating said imager and sent to said camera control unit;	 FIG.1 Asaida 782 (Figure 1) "[W]ith the present video camera unit, the two-line-concurrent three-color imaging output signals S_{RO}, S_{RE}, S_{GO}, S_{GE}, S_{BO} and S_{BE}, obtained by the solid-state image sensors 2R, 2G, and 2B, are changed by the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE into two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}. The two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, are converted by the P/S converter 7 into serial data as the camera output data $HEAD_{OUT}$, which are serially outputted at the serial input/output port 10 by means of the encoder/decoder 9." (Asaida 782 at 5:50-61.)	connected, and to this timing generator 16, an NTSC crystal oscillator 17, a PAL crystal oscillator 18, and a switching device 19 are provided. Furthermore, a first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU 20, either of the oscillators 17, 18 is selected." (Okada 852 at 4:4-15.)  Okada 852 (Figure 1) "A first example is configured like the above, and in the example, each television system can be selected by selective switches arranged at the processor or the like, and the state of selection of the switches can be grasped by the second CPU 26. Then, this second CPU 26 reads out the setting data of the selected system from the ROM 27 to set the processing contents of each circuit by this setting data. At the same time,

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Claims	**Asaida 782**	**in combination with one or more of the following references**
	"[T]he synchronizing circuit block 19 is supplied with a reference synchronizing signal $GENLOCK_{REF}$ for generator locking through synchronizing input terminal 27, while the control circuit block 20 is supplied with a control signal CTL through a control input terminal 28." (Asaida 782 at 7:16-21.) "The encoder/decoder 9 encodes the serial data supplied from P/S converters 7 and 31 and serially transmits the encoded serial data via the serial input/output port 10 to a camera control unit CCU described below, while also decoding various serial data transmitted from the camera control unit CCU to the serial input/output port 10, such as return video signals D_{RET}, prompter signals D_{PROMPT}, output signals CCU_{OUT} from the camera control unit CCU or control data D_{CTL}." (Asaida 782 at 7:35-43.) Thus, encoder/decoder 9 transmits either a separate timing signal or a timing signal embedded in the serial data signal received from P/S converter 7 (which originated from image sensors 2R, 2G, and 2B) and sent to the CCU through input/output port 10.	the information of the selected system is also transmitted to the first CPU 20 on the scope side from this second CPU 26, and on this scope side, the selected setting data is read out from the ROM 21 by the first CPU 20 to set the processing contents of each circuit, and further, either of the above oscillators 17, 18 is selected and set." (Okada 852 at 4:58-5:3.) "That is, if the NTSC system is selected, the NTSC system oscillator 17 is connected to the timing generator 16 by the switching circuit 19. In this timing generator 16, the oscillating signal with, for example, a frequency of 14.32 MHz generated in the oscillator 17 is divided to form the horizontal synchronization signal with a frequency of 15.734 kHz (fh1) and the vertical synchronization signal with a frequency of 59.94 Hz, and the driving pulse based on this is given to the CCD 1. Then, the picture signal extracted from this CCD 1 is subjected to the digital conversion after passing through the AGC circuit 5 for performing the correlative double sampling and the amplification processing, and as shown in FIG. 2, this digital picture signal is subjected to a specified processing by the DSP circuit 22, and it is supplied to the memory section 24 on the processor side." (Okada 852 at 5:4-20.)

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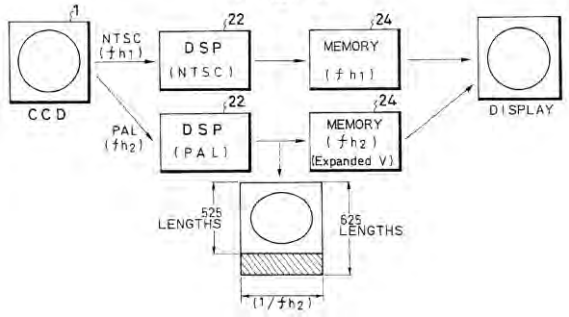
Claims	**Asaida 782**	**in combination with one or more of the following references**
		Fig. 2  Okada 852 (Figure 2) "In this memory section 24, the picture data is written in the imaging memory 24A in the timing of the synchronization signal formed in the timing generator 16, and after that, this picture data is read out in the same timing to be stored in the display memory 24B (as the data corresponding to the number of scanning lines of 525). The data of this display memory 24 is converted into the signals of R, G, and B from the brightness signal and the color difference signal in the Y/C matrix circuit 25 after being converted to the analog signal in the D/A converter 11. Then, each of these signals of R, G, and B is outputted to a monitor of the NTSC system through the isolation device 29 and the buffers 30 (A to C), and consequently, a picture of the NTSC system is displayed on the monitor." (Okada 852 at 5:21-35 (emphasis added).) Thus, the timing signal actuates the imager and is sent to the CCU. "The sensor 20 is controlled by the timing generator

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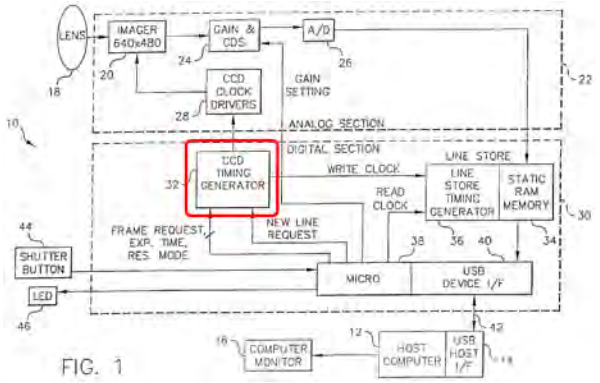
Claims	**Asaida 782**	**in combination with one or more of the following references**
		32 via the CCD clock driver 28. The timing generator 32 has a control input for receiving a new line request signal from the microprocessor 38; the new line request signal thus initiates the generation of clock signals to output a new line from the sensor 20. The digital data from the sensor 20 is temporarily stored in the static RAM line store memory 34, preferably a 64K bit static RAM memory (for example part number IDT7164 made by Integrated Device Technology, Inc.) which is controlled by a line store timing generator 36 so as to serve as a line store. Besides controlling the sensor 20, the CCD timing generator 32 also controls the line store write clock applied to the line store timing generator 36." (Endsley 471 at 3:24-36.) "The output of the line store memory 34 is connected to the host computer 12 via the USB device interface 40, which operates at a maximum data rate of 12M bits/sec." (Endsley 471 at 3:37-39.)  FIG. 1

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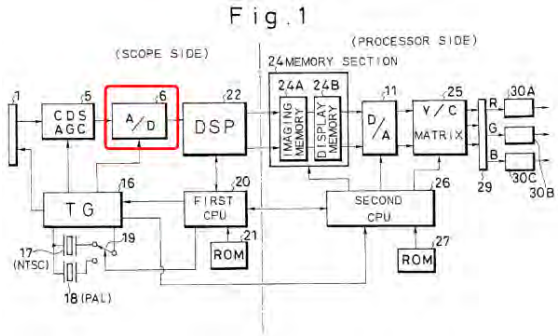
Claims	**Asaida 782**	**in combination with one or more of the following references**
		Endsley 471 (Figure 1) The USB Device 40 transmits either a separate timing signal (*see, e.g.*, Section 5.10.2 of USB Spec. Rev. 1.0) or a timing signal embedded in the serial data signal sent to the CCU.
a converter, for converting the analog stream of video data into the stream of digital video data;	"The two-line-concurrent three-color imaging output signals S_{RO}, S_{RE}, S_{GO}, S_{GE}, S_{BO} and S_{BE}, processed for level adjustment by the level adjustment circuits 4RO, 4RE, 4GO, 4GE, 4BO and 4BE, are transmitted by means of low-pass filters 5RO, 5RE, 5GO, 5GE, 5BO and 5BE, respectively, to A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, functioning as analog/ digital converting means, respectively." (Asaida 782 at 5:14-22.) "A driving clock CK_{AD} having a frequency four times the frequency of the color subcarrier frequency f_{SC}, or $4f_{SC}$, is supplied to the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, by means of a timing generator, not shown. The A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE digitize the two-line-concurrent three-color imaging output signals S_{RO}, S_{RE}, S_{GO}, S_{GE}, S_{BO} and S_{BE} with the $4f_{sc}$ driving clock CK_{AD} to produce two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, respectively. The two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, produced by the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, are supplied to a parallel/serial converter (P/S converter) 7 and to a signal processing section 8." (Asaida 782 at 5:23-37.)	"[T]o the CCD 1, an AGC (automatic gain control) circuit including a CDS (correlative double sampling) circuit is connected similarly to that in the prior art, and to this AGC circuit 5, a DSP (digital signal processor) circuit 22 is connected through an A/D converter 6." (Okada 852 at 4:29-33.) Fig. 1  Okada 852 (Figure 1) "An analog section 22 in the camera 10 includes the sensor 20, a CDS/gain block 24 for performing correlated double sampling (CDS) and setting the analog gain, an analog-to-digital (A/D) converter 26 for converting the analog output

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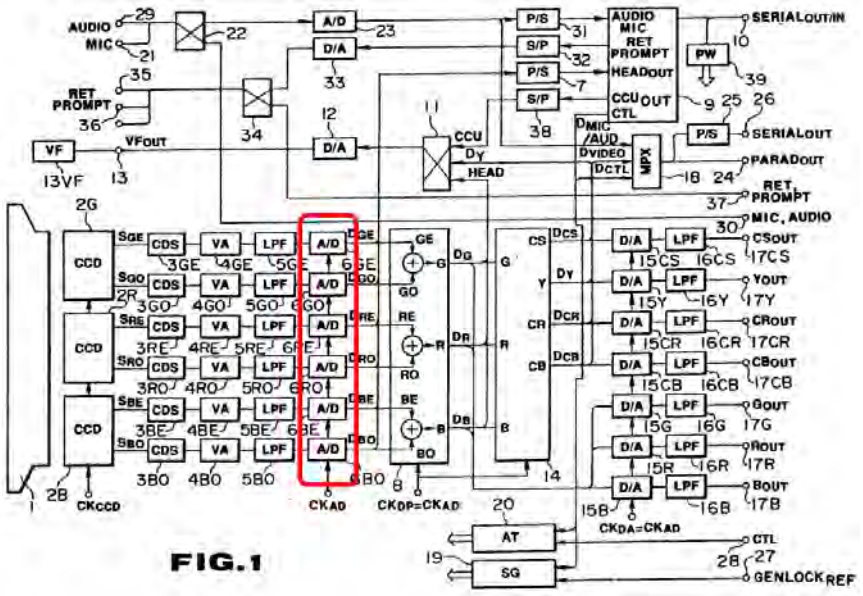
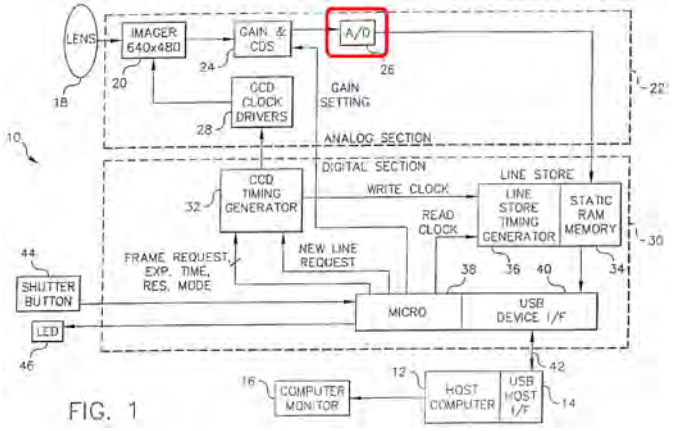
Claims	**Asaida 782**	**in combination with one or more of the following references**
	 FIG.1 Asaida 782 (Figure 1)	signal from the CCD sensor 20 to, e.g., an 8-bit digital signal, and CCD clock drivers 28 for clocking the sensor 20." (Endsley 471 at 3:13-18.)  FIG. 1 Endsley 471 (Figure 1) "Reference is now made to FIG. 4, which is an schematic block diagram of the miniature endoscope according to a preferred embodiment of the present invention. Parts that are identical to those shown above are given the same reference numerals and are not referred to again except as necessary for an understanding of the present embodiment. Optical assembly 48 receives light, indicated by arrows 60, from an object being viewed. The light is processed by optical assembly 48, as will be explained below, to reach image sensor 46 were it is converted from photons into electrical signals. The electrical signals are digitized and passed to a

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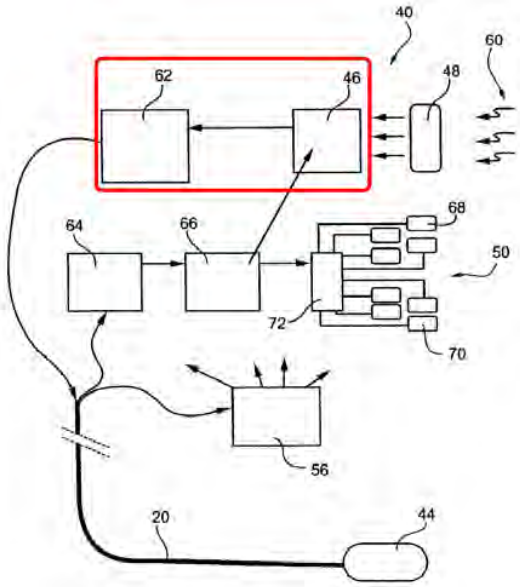
Claims	**Asaida 782**	**in combination with one or more of the following references**
		transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Adler 940 at 10:7-19 (emphasis added).)  Adler 940 (Figure 4) Because "the electrical signals are digitized and passed to a transmitting device 62" in the camera head, the camera head must contain a converter for converting an analog stream of video data into a stream of digital video data. "One of the advantages of CMOS image sensors (CMOS

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		imagers) over CCD imagers is that the CMOS imager chip can include digital signal processing circuitry. In practice, the signal processing is more often performed on a companion chip, in order to provide greater application flexibility. However, CMOS imagers often have integrated analog to digital converters to convert the analog signal to a digital bit stream that can be processed by the companion chip. The digitized information then must be transferred to companion chip or other external devices for picture storage, processing, or transmission." (Chung 290 at 1:17-27 (emphasis added).) "FIG. 4 illustrates CMOS video imaging sensing circuitry according to the preferred embodiment disclosed in co-pending U.S. application Ser. No 09/062,343. This circuitry includes a CMOS image sensor chip 50 and an image processor chip 52. The CMOS image sensor chip 50 typically includes a number of light responsive CMOS pixel sensors which develop analog signals representative of an image. These analog signals are then A to D converted by the ADC circuit to form digital signals Din0, Din1 . . . Dinn. The image processor chip 52 includes a data processor 53 which performs various manipulations of the image data such as compression and color processing. The processor 53 may be software driven or a hardware embodiment." (Chung 290 at 2:14-26.)

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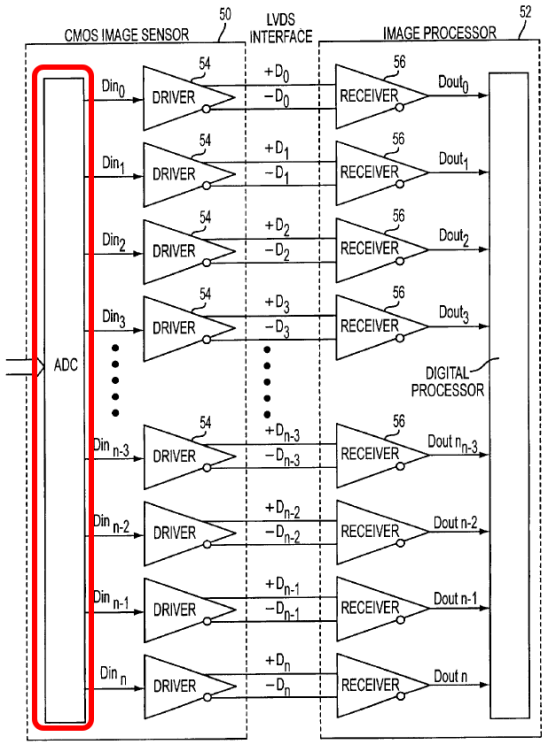
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Chung 290 (Figure 4)
a serializer, for serializing the stream of digital video data	"A driving clock CK_{AD} having a frequency four times the frequency of the color subcarrier frequency f_{SC}, or $4f_{SC}$, is supplied to the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, by means of a timing generator, not shown. The A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE digitize the two-line-concurrent three-color imaging output signals S_{RO}, S_{RE}, S_{GO}, S_{GE}, S_{BO} and S_{BE} with the $4f_{sc}$	To the extent this element is not expressly disclosed, it is inherent in Endsley 471 by virtue of disclosing and claiming USB as a communications medium. Specifically, section 10.2.2 of the USB Specification Revision 1.0 (Jan. 15, 1996) explains that "[t]he actual

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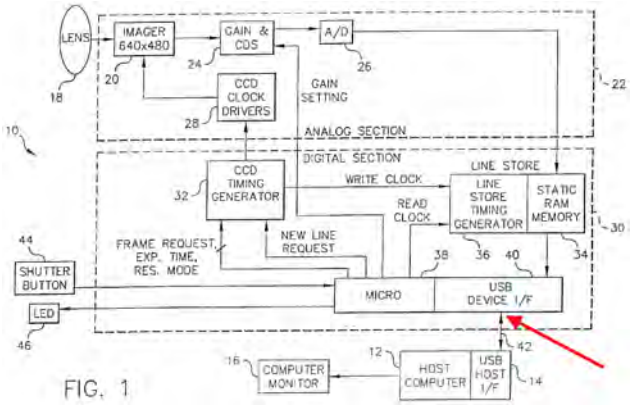
Claims	**Asaida 782**	**in combination with one or more of the following references**
for transmission over said cable;	driving clock CK_{AD} to produce two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, respectively. The two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, produced by the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, are supplied to a parallel/serial converter (P/S converter) 7 and to a signal processing section 8." (Asaida 782 at 5:23-37.) "The P/S converter 7 changes the two-line-concurrent digital three color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, supplied from the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO, and 6BE, from parallel data into serial data. The serial data, produced by the P/S converter 7, are supplied as camera output data $HEAD_{OUT}$ to a light-transmitting encoder/decoder 9." (Asaida 782 at 5:38-44.) "The encoder/decoder 9 encodes the serial data, that is, the camera output data $HEAD_{OUT}$, supplied from the P/S converter 7, and outputs the encoded data at a serial input/output port 10 over an optical fiber cable, not shown." (Asaida 782 at 5:45-49.)	transmission of data across the physical USB takes place as a serial bit stream. A Serial Interface Engine (SIE), whether implemented as part of the host or a USB device, handles the serialization and deserialization of USB transmissions. On the host, this SIE is part of the host controller." (USB Spec. Rev. 1.0 at 200.) Thus, in order for USB to be implemented as disclosed and claimed in Endsley 471, there must be "a serializer, for serializing the stream of digital video data for transmission over said cable."  Endsley 471 (Figure 1) "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system

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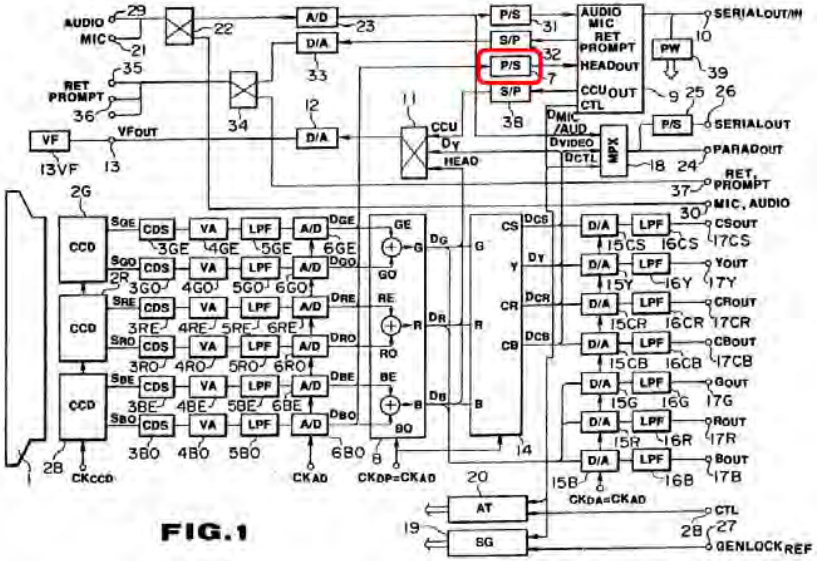
Claims	**Asaida 782**	**in combination with one or more of the following references**
	 FIG.1 Asaida 782 (Figure 1)	including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope. The skilled person will appreciate that the wire connection 20 may be an optical connection or may instead use RF or a like means of wireless communication. The miniature endoscopic front-end 10 may be designed for connection to any standard PC input (the USB input for example)." (Adler 940 at 9:24-38 (emphasis added).) "Reference is now made to FIG. 4, which is an schematic block diagram of the miniature endoscope according to a preferred embodiment of the present invention. Parts that are identical to those shown above are given the same reference numerals and are not referred to again except as necessary for an understanding of the present embodiment. Optical assembly 48 receives light, indicated by arrows 60, from an object being viewed. The light is processed by optical assembly 48, as will be explained below, to reach image sensor 46 were it is converted from photons into electrical signals. The electrical signals are digitized and passed to a transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Adler 940 at 10:7-19 (emphasis added).) Because both USB and LVDS are contemplated by Adler

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		940 as a means for transmitting the stream of digital video data over cable 20, both of which are serial communication protocols, the camera head must include a component that a serializes the digital video data.
at least one digital serial driver;	"The encoder/decoder 9 encodes the serial data, that is, the camera output data $HEAD_{OUT}$, supplied from the P/S converter 7, and outputs the encoded data at a serial input/output port 10 over an optical fiber cable, not shown." (Asaida 782 at 5:45-49.) To the extent this element is not expressly disclosed, it is inherent in Asaida 782. It would be within the knowledge of one of ordinary skill in the art at the time of the alleged invention that transmitting a serial digital signal over a cable would necessarily require a driver to drive the signal and a receiver to receive the signal. Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005) (citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)). Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	To the extent this element is not expressly disclosed, it is inherent in Endsley 471 by virtue of disclosing and claiming USB as a communications medium. Specifically, section 7.1.1 of the USB Specification Revision 1.0 is directed to "USB Driver Characteristics": "The USB uses a differential output driver to drive the USB data signal onto the USB cable. The static output swing of the driver in its low state must be below the VOL of 0.3 V with a 1.5 kW load to 3.6 V and in its high state must be above the VOH of 2.8 V with a 15 kW load to ground as listed in Table 7-4. The output swings between the differential high and low state must be well balanced to minimize signal skew. Slew rate control on the driver is required to minimize the radiated noise and cross talk. The driver's outputs must support three-state operation to achieve bi-directional half duplex operation. High impedance is also required to isolate the port from downstream devices that are being hot inserted or which are connected but powered down. The driver must tolerate a voltage on the signal pins of -0.5 V to 3.8 V with respect to local ground reference without damage. It must tolerate this voltage for 10.0 μs while the driver is active and driving, and tolerate the

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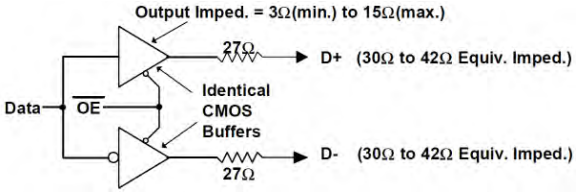
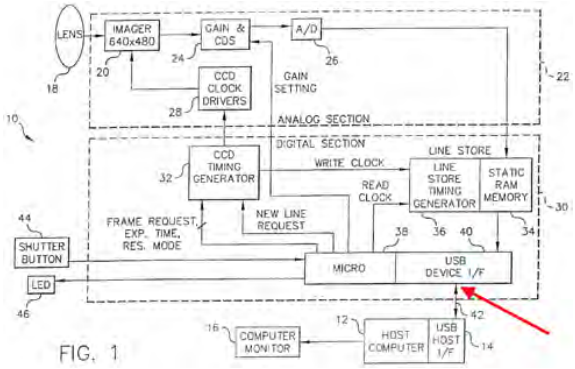
Claims	**Asaida 782**	**in combination with one or more of the following references**
		condition indefinitely when the driver is in its high impedance state." (USB Spec. Rev. 1.0 at 111-13.)  USB Spec. Rev. 1.0 (Figure 7-1)  FIG. 1 Endsley 471 (Figure 1) "Reference is now made to FIG. 4, which is an schematic block diagram of the miniature endoscope according to a preferred embodiment of the present invention. Parts that are identical to those shown above are given the same reference numerals and are not referred to again except as necessary for an understanding of the present embodiment. Optical

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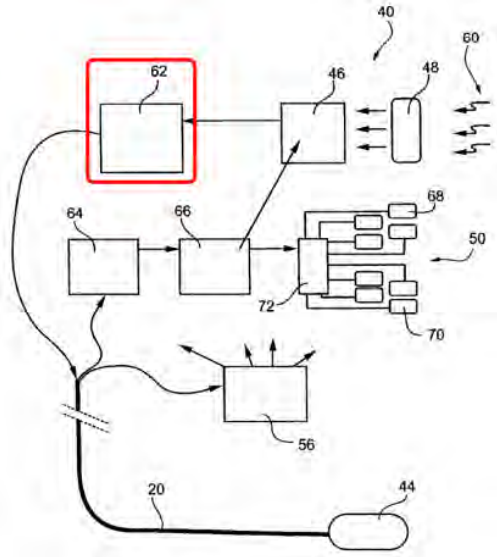
Claims	**Asaida 782**	**in combination with one or more of the following references**
		assembly 48 receives light, indicated by arrows 60, from an object being viewed. The light is processed by optical assembly 48, as will be explained below, to reach image sensor 46 were it is converted from photons into electrical signals. The electrical signals are digitized and passed to a transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Adler 940 at 10:7-19 (emphasis added).)  Adler 940 (Figure 4) ***Alternatively***, this limitation is met if USB is used, rather than LVDS, as a communications medium between the

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		endoscope 10 and processing device 30 as contemplated by the following disclosure. "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope. The skilled person will appreciate that the wire connection 20 may be an optical connection or may instead use RF or a like means of wireless communication. The miniature endoscopic front-end 10 may be designed for connection to any standard PC input (the USB input for example)." (Adler 940 at 9:24-38 (emphasis added).) A driver would necessarily be required to drive a USB signal over wire connection 20. To the extent this element is not expressly disclosed, it is inherent in Adler 940. Specifically, section 7.1.1 of the USB Specification Revision 1.0 is directed to "USB Driver Characteristics": "The USB uses a differential output driver to drive the USB data signal onto the USB cable. The static output swing of the driver in its low state must be below the VOL of 0.3 V

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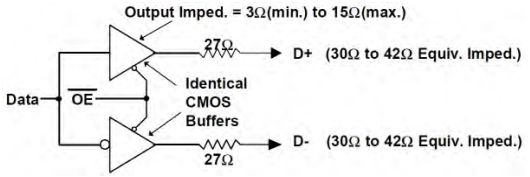
Claims	**Asaida 782**	**in combination with one or more of the following references**
		with a 1.5 kW load to 3.6 V and in its high state must be above the VOH of 2.8 V with a 15 kW load to ground as listed in Table 7-4. The output swings between the differential high and low state must be well balanced to minimize signal skew. Slew rate control on the driver is required to minimize the radiated noise and cross talk. The driver's outputs must support three-state operation to achieve bi-directional half duplex operation. High impedance is also required to isolate the port from downstream devices that are being hot inserted or which are connected but powered down. The driver must tolerate a voltage on the signal pins of -0.5 V to 3.8 V with respect to local ground reference without damage. It must tolerate this voltage for 10.0 µs while the driver is active and driving, and tolerate the condition indefinitely when the driver is in its high impedance state." (USB Spec. Rev. 1.0 at 111-13.)  USB Spec. Rev. 1.0 (Figure 7-1) "TIA/EIA-644, otherwise known as LVDS, is a signaling method used for high-speed, low-power transmission of binary data over copper. This signaling technique uses lower output-voltage levels than the 5-V differential standards (such as TIA/EIA-422B) to reduce power consumption,

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		increase switching speed, and allow operation with a 3.3-V supply rail. The LVDS current-mode drivers create a differential voltage (250 mV to 450 mV) across a 100-Ω load. The LVDS receiver detects signals as low as ±100 mV with as much as ±1-V ground noise. The standard specifies a recommended maximum data rate of 655 Mbit/s (and a theoretical maximum of 1.923 Gbit/s on a lossless line)." (TI LVDS at 1.) "The intended application of this signaling technique is for baseband data transmission over controlled impedance media of approximately 100 Ω, where the transmission media may be printed circuit board (PCB) traces, backplanes, or cables." (TI LVDS at 1.) "Figure 1 shows a typical connection with LVDS drivers and receivers."

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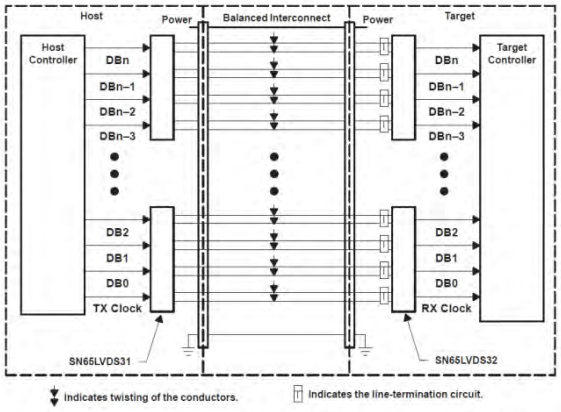
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Figure 1. Typical Connection With LVDS Drivers and Receivers TI LVDS (Figure 1) "The LVDS driver produces a differential voltage across a 100-Ω load in the range of 247 mV to 454 mV with a typical offset voltage of 1.2 V relative to ground (see Figure 2). Most drivers are commonly implemented as current-mode devices, which allow frequency to be virtually independent of power consumption. These two characteristics, low voltage swings and constant current, allow LVDS drivers to operate at higher data rates and lower power dissipation." (TI LVDS at 2.) "As the need for higher bandwidth accelerates, system designers are choosing differential signaling to satisfy high bandwidth requirements while reducing power, increasing noise immunity, and decreasing EMI emissions. LVDS is a low swing, differential signaling technology providing very

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		fast data transmission, common-mode noise rejection, and low power consumption over a broad frequency range. The Virtex-E family delivers the programmable industry's highest bandwidth and most flexible differential signaling solution for direct interfacing to industry-standard LVDS devices." (Virtex-E LVDS at 1.) "With up to 36 I/O pairs operating at 622 Megabits per second (Mb/s) or up to 344 I/O pairs operating at over 311 Mb/s, the Virtex-E family supports multiple 10 Gb/s ports while maintaining high signal integrity with low power consumption. Unlike other PLD solutions, all Virtex-E LVDS I/Os support input, output, and I/O signaling, providing a system designer unparalleled flexibility in board layout." (Virtex-E LVDS at 1.) Advantages of LVDS include: "• LVDS is specified to be technology and process independent. • LVDS is EMI tolerant. Common-mode noise is equally removed by two conductors and rejected by the receiver. • No transmission medium is defined in the standard. The medium can be tailored to meet the specific application requirements. • The typical LVDS voltage swing is 350 mV, resulting in a higher transfer rate and lower power consumption." (Virtex-E LVDS at 2.) "There are two configurations that are used in LVDS applications, point-to-point and multi-drop. The Virtex-E

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		family supports both LVDS configurations. **Point-to-Point** In point-to-point configuration, there is one transmitter and one receiver. The LVDS driver is a current source that drives a differential pair of lines. The typical current drive is 3.5 mA. The receiver has high DC impedance. The majority of the driver current flows across the termination resistor generating about 350 mV at the receiver inputs (Figure 1). **Multi-Drop** A multi-drop LVDS configuration has one transmitter and multiple receivers. The differential termination resistor is placed close to the last receiver (Figure 3)." (Virtex-E LVDS at 2.) Among the many applications that LVDS is suited for are "digital cameras" and "multimedia peripherals." (Virtex-E LVDS at 2-3.) "Figure 1 shows the schematic of a standard LVDS driver driving the Virtex-E receiver. An LVDS driver drives the two 50 W transmission lines into a Virtex-E LVDS receiver. The two 50 W single-ended transmission lines can be micro-strip, strip-line, a 100 W differential twisted pair, or a similar balanced differential transmission line." (Virtex-E LVDS at 3.)

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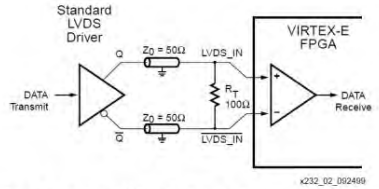
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 **Figure 1: A Standard LVDS Driver Driving a Virtex-E LVDS Receiver** <u>Virtex-E LVDS (Figure 1)</u> "As may be seen, the circuit of FIG. 4 employs a plurality of LVDS circuits 11. Each circuit 11 includes a respective driver 54 and a respective receiver 56. Each driver 54 receives a respective input signal Din0, Din1 . . . Dinn, which are digital logic levels of, for example, 3.3 volts for logic "1" and zero volts for logic "0". Changes in state in these signals are transmitted over the differential lines to the respective receivers 56. Each receiver 56 generates a respective output signal Dout0, Dout1, . . . Doutn, which are at the several hundred millivolt level." (Chung 290 at 2:27-36.)

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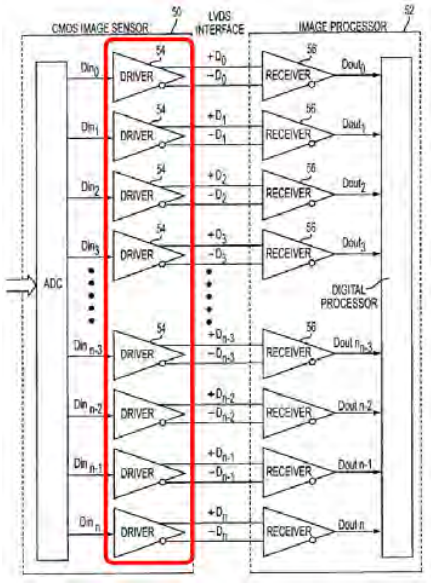
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Chung 290 (Figure 4)
a processor; and	"The signal processing section 8 adds the two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, supplied from the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, for each of the color signals, in such a manner that switching between upper and lower lines on both sides of a center line is done on a field-by-field basis to form interlaced digital three-color signals D_R, D_G and D_B. The signal processing section 8 also processes the digital three color signals D_R, D_G and D_B using, for example, gamma correction and image enhancement." (Asaida 782 at 5:62-6:4.)	"In FIG. 1 and FIG. 2, the circuit configuration of an electronic endoscope according to the embodiment is shown. In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having a number of scanning lines or the like suitable for the scanning line of the NTSC system, and to this CCD 1, a timing generator 16 is connected, and to this timing generator 16, an NTSC crystal oscillator 17, a PAL crystal oscillator 18, and a switching device 19 are provided. Furthermore, a first CPU 20 is provided, which controls the total while controlling this

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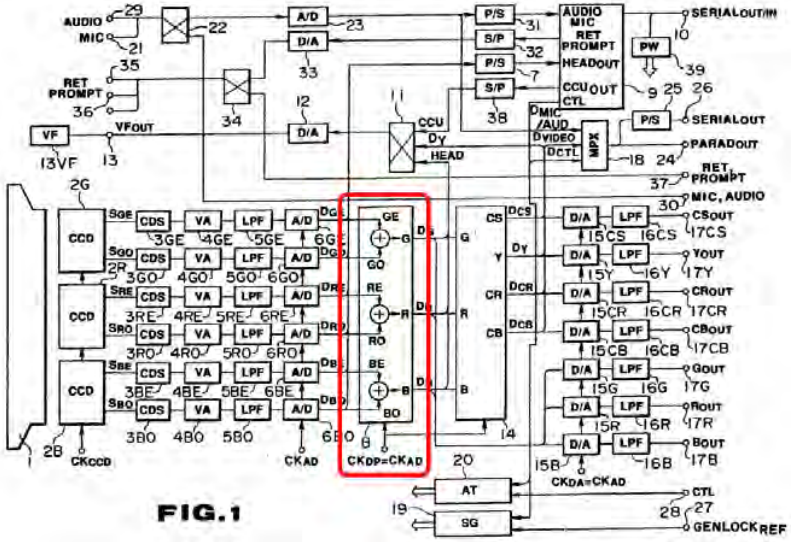
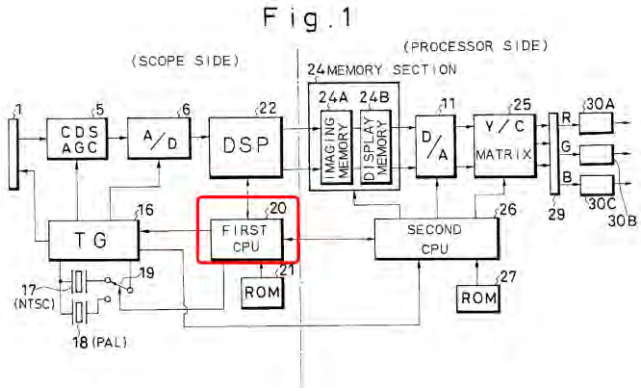
Claims	**Asaida 782**	**in combination with one or more of the following references**
	 FIG.1 Asaida 782 (Figure 1) Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005) (citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)). Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the	switching device 19, and by the control of this first CPU 20, either of the oscillators 17, 18 is selected." (Okada 852 at 4:4-15.)  Okada 852 (Figure 1) "A digital section 30 includes a CCD timing generator 32, a static RAM line store memory 34, a line store timing generator 36, a microprocessor 38, and a USB device interface 40." (Endsley 471 at 3:19-22.) "The USB interface 40, which may be incorporated as part of the microprocessor 38, such as the Intel 82930 microprocessor, reads data from the line store 34." (Endsley 471 at 3:43-46.)

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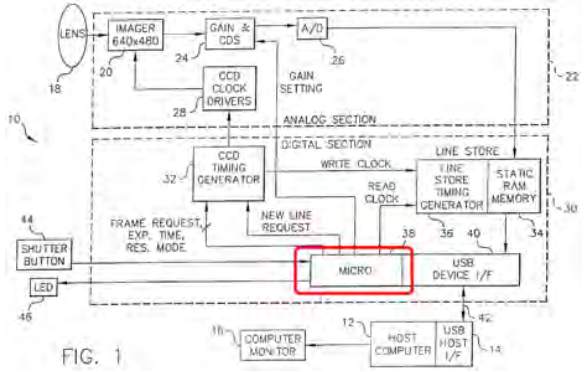
Claims	**Asaida 782**	**in combination with one or more of the following references**
	alleged invention of the '310 patent.	 Endsley 471 (Figure 1) "As shown in FIG. 1, camera processor 14 includes a microprocessing unit ("MPU") 48, a CCD driver 50, and signal processing ("SP") circuitry 52. In operation, MPU 48 provides control to CCD driver 50 for transmitting driving signals to CCD 18 in camera head 12. In response to the driving signals, CCD 18 produces electrical signals representing an image of objects within the field of view of CCD 18, and transmits the electrical signals to signal processing circuitry 52. Signal processing circuitry 52 processes the electrical signals from CCD 18 and converts them to video signals for displaying the image on video monitor 20." (Dowdy 082 at 4:60-5:3.)

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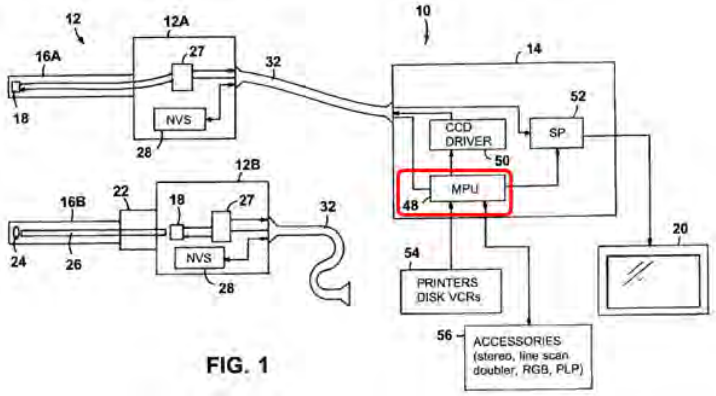
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 FIG. 1 Dowdy 082 (Figure 1) "Referring also to FIG. 3, MPU 48 uses the information stored in NVS 28 to control the operation of CCD driver 50 and signal processing circuitry 52. When the user connects cable 32 of camera head 12 to camera processor 14, and, if necessary, powers up video endoscopy system 10, MPU 48 detects the connection and responds by downloading the information from NVS 28 into a memory 58, such as a RAM, of MPU 48 (step 200). MPU 48 reads the stored information out of NVS 28 through a serial data link in cable 32 that includes a CLOCK line 60 controlled by MPU 48 and a DATA line 62 that is shared by NVS 28 and MPU 48." (Dowdy 082 at 5:9-19.) "MPU 48 communicates with signal processing circuitry 52 through a bidirectional serial data link that includes a CLOCK line 80 controlled by MPU 48 and a DATA line 82

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		that is shared by MPU 48 and signal processing circuitry 52. MPU 48 also controls an ENABLE line 84 that activates external control of signal processing circuitry 52." (Dowdy 082 at 6:1-6.) "After modifying the values of table entries 72-78 received from signal processing circuitry 52, MPU 48 transmits the updated values to signal processing circuitry 52 (step 218). When entries from NVS 28 reflect replacement values for entries in lookup table 68, MPU 48 transmits the replacement values (step 218) without requesting values from signal processing circuitry and modifying those values (steps 208-216)." (Dowdy 082 at 6:18-25.) "After signal processing circuitry 52 receives the updated values from MPU 48 (step 220), signal processing circuitry 52 uses the updated values in processing the electrical signals from CCD 18 for display on video monitor 20 (step 222). That is, signal processing circuitry 52 uses the updated values in locations 69—rather than the nominal values from lookup table 68—in performing the conversion of the electrical signals from CCD 18 to video signals." (Dowdy 082 at 6:26-33.) "Referring to FIG. 4, in a more detailed view, camera head 12 includes CCD 18 (located, as discussed, either in the head or at the tip of the endoscope), NVS 28 and a set of button switches 92 for system control, and camera processor 14 includes a camera controller 94 and a signal processor 96. Cable 32, which connects camera head 12 to camera

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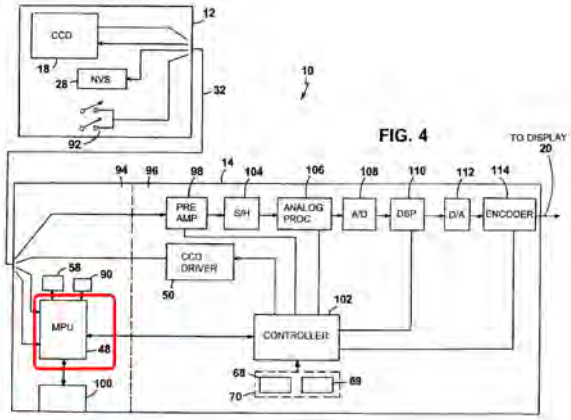
Claims	**Asaida 782**	**in combination with one or more of the following references**
		processor 14, carries drive signals from CCD driver 50 in signal processor 96, electrical signals from CCD 18 to a preamplifier 98 in signal processor 96, data between NVS 28 and MPU 48 in camera controller 94, and signals from button switches 92 to MPU 48." (Dowdy 082 at 6:48-58.)  Dowdy 082 (Figure 4) "MPU 48 controls signal processor 96 in response to signals from button switches 92 and signals from controls in a front panel 100 of camera controller 94. The controls in front panel 100 allow the user of video endoscopy system 10 to configure button switches 92 to perform desired functions. Thus, for example, button switches 92 could be configured to cause signal processor 96 to pause the video image displayed at video monitor 20 (FIG. 1). MPU 48 also displays system parameters at front panel 100, interacts with NVS 28 by

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		downloading information about camera head 12 and updating run time information in NVS 28, updates signal processing parameters in light of the information about camera head 12, and communicates with signal processor 96, all as discussed above." (Dowdy at 6:59-7:5.) Although MPU 48 is located in camera processor 14, it is contained within camera controller 94 which is independent of camera processor 96. Because camera controller 94 and camera processor 96 are independent units housed within camera processor 14, camera controller 94 (and as a result, MPU 48) could have been located in camera head 12. Locating camera controller 94 in the camera head 12 would have been a design option attractive to one of ordinary skill in the art looking to minimize communication circuitry between NVS 28 and MPU 48, as both would be housed within camera 12. "A regulator 19, a programmable nonvolatile memory 20, a CPU 21, a selector (SEL) 22, a supply voltage detector 23, a scope switch 24, and a connector 25 are arranged behind the rear end of the insertion unit 11 of the endoscope 2. The regulator 19 converts a CCD driving voltage fed from a CCD driving power supply 18 incorporated in the image processing apparatus 3A into a desired voltage. The programmable nonvolatile memory 20 in which the endoscope-related data is stored is realized with an EEPROM, a flash ROM, an FRAM, or an MRAM." (Oshima 212 at 6:54-63.) "The CPU 21 includes a one-chip microcomputer for

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		performing a plurality of arithmetic operations including communication and writing, or reading. Specifically, the CPU 21 transmits or receives the endoscope-related data to or from the image processing apparatus 3A through a serial interface, and writes or reads the endoscope-related data in or from the nonvolatile memory 20. The CPU 21 includes a ROM, a RAM, a watchdog timer (WDT), a serial controller (S10), a parallel controller (P10), and a counter (CTC). The selector 22 acts as a serial interface means for transmitting or receiving the endoscope-related data over a sole signal line 49. The supply voltage detector 23 detects a fluctuation or drop in supply voltage and outputs a reset signal, thus preventing a malfunction of the CPU 21 or the nonvolatile memory 20." (Oshima 212 at 6:63-7:10.)

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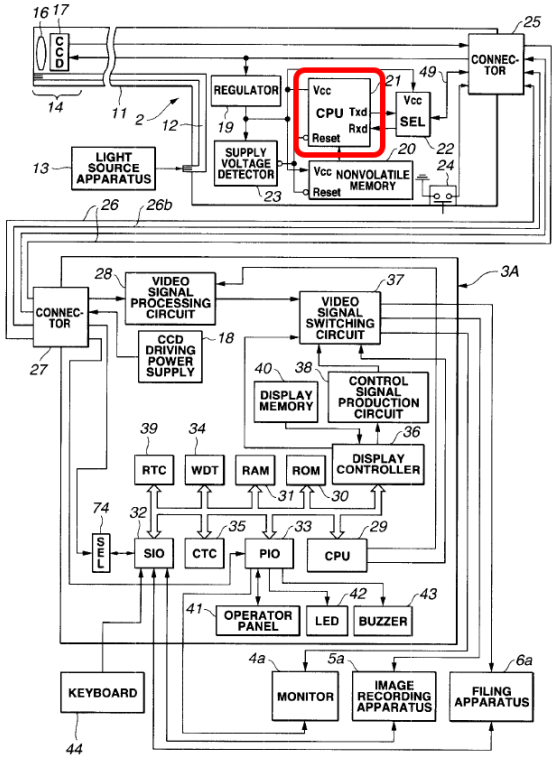
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Oshima 212 (Figure 2)
a memory device, accessible by said processor, containing	Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005) (citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir.	"In FIG. 1 and FIG. 2, the circuit configuration of an electronic endoscope according to the embodiment is shown. In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having a number of scanning lines or the like suitable for the scanning line of the NTSC system, and to this CCD 1, a timing generator 16 is

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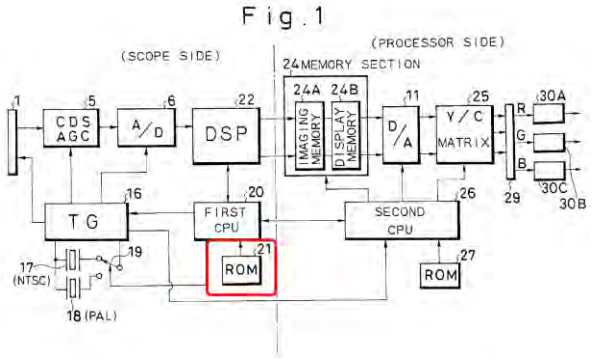
Claims	**Asaida 782**	**in combination with one or more of the following references**
camera head information;	2000)). Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	connected, and to this timing generator 16, an NTSC crystal oscillator 17, a PAL crystal oscillator 18, and a switching device 19 are provided. Furthermore, a first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU 20, either of the oscillators 17, 18 is selected." (Okada 852 at 4:4-15.)  Okada 852 (Figure 1) "The NTSC crystal oscillator 17 generates a signal with a frequency of about 14.32 MHz (N·fh1), and the PAL oscillator 18 on the other side may be an oscillator which generates a signal with the above mentioned frequency of about 17.73 MHz, but in this example, an oscillator which generates a signal with a frequency of N·fh2 [N times the frequency of the horizontal synchronization signal of 15.625 kHz (=fh2)] near the NTSC oscillation frequency is used. Consequently, the change of the circuit member relating to

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		the drive operation, the setting of a constant, or the like become easy. Moreover, to the first CPU 20, a ROM 21 storing setting data for the control meeting the NTSC system or the PAL system is connected." (Okada 852 at 4:16-28 (emphasis added).) "A first example is configured like the above, and in the example, each television system can be selected by selective switches arranged at the processor or the like, and the state of selection of the switches can be grasped by the second CPU 26. Then, this second CPU 26 reads out the setting data of the selected system from the ROM 27 to set the processing contents of each circuit by this setting data. At the same time, the information of the selected system is also transmitted to the first CPU 20 on the scope side from this second CPU 26, and on this scope side, the selected setting data is read out from the ROM 21 by the first CPU 20 to set the processing contents of each circuit, and further, either of the above oscillators 17, 18 is selected and set." (Okada 852 at 4:58-5:3 (emphasis added).) "A digital section 30 includes a CCD timing generator 32, a static RAM line store memory 34, a line store timing generator 36, a microprocessor 38, and a USB device interface 40." (Endsley 471 at 3:19-22.) "The output of the line store memory 34 is connected to the host computer 12 via the USB device interface 40, which operates at a maximum data rate of 12M bits/sec. (See the article 'Universal Serial Bus to Simplify PC I/O', by Michael

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		Slater in Microprocessor Report, Volume 9, Number 5, Apr. 17, 1995 for more detail about the benefits of the USB interface.) The USB interface 40, which may be incorporated as part of the microprocessor 38, such as the Intel 82930 microprocessor, reads data from the line store 34." (Endsley 471 at 3:37-46.) "[T]he present invention includes a novel way of 'line throttle clocking' the image sensor 20 by varying a line blanking interval 68 from line to line, as shown in FIG. 5, so as to transfer lines of data from the CCD image sensor 20 into the line store memory 34 at the appropriate time." (Endsley 471 at 4:54-59.) "FIG.5 shows that, once the image data is transferred by the readout pulse 60 to the light-protected vertical registers 50, the line clocking is 'throttled' to accommodate the storage capacity of the line store memory 34. The line store memory 34 is capable of storing a small number of lines of data and provides block transfer capability at low cost. Whenever the line store memory 34 has sufficient room to accommodate a new line of image data, the timing generator 32 creates the vertical and horizontal timing pulses 62 and 64 needed to read out the next line from the image sensor, as shown in FIG. 5, and then returns to a wait state until sufficient data is transferred from the line store memory 34 to the computer 12 so as to provide room for the next line. Since the waiting period (equal to the line blanking time) depends on the USB bus traffic, the line readout times and frame readout times are variable, rather than fixed, as in prior art cameras." (Endsley

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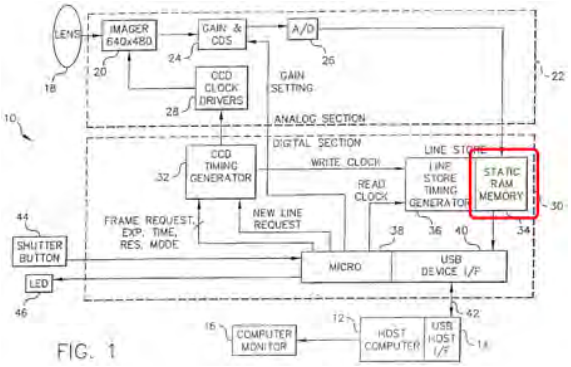
		471 at 4:60-5:9.)  FIG. 1 Endsley 471 (Figure 1) ***Alternatively***, this limitation is met by memory in the USB device interface that contains information related to USB descriptors. "The USB interface 40 . . . may be incorporated as part of the microprocessor 38, such as the Intel 82930 microprocessor." (Endsley 471 at 3:43-45.) "USB devices report their attributes using descriptors. A descriptor is a data structure with a defined format. Each descriptor begins with a byte-wide field that contains the total number of bytes in the descriptor followed by a byte-wide field that identifies the descriptor type. "Using descriptors allows concise storage of the attributes of individual configurations because each configuration may

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		reuse descriptors or portions of descriptors from other configurations that have the same characteristics. In this manner, the descriptors resemble individual data records in a relational database." (USB Spec. Rev. 1.0 at 181.) "A device descriptor describes general information about a USB device. It includes information that applies globally to the device and all of the device's configurations. A USB device has only one device descriptor." (USB Spec. Rev. 1.0 at 182.) "An apparatus sends electrical signals that represent an optical image to a processor for conversion to video signals suitable for display on a display device. The apparatus includes a device for insertion into a region to be viewed for developing an optical image of the region, an imager for generating electrical signals that represent the optical image, and a digital memory for storing information about the imager. The device is adapted to be connected to the processor so that the processor can receive the electrical signals from the imager and obtain information from the digital memory. The processor uses the information from the digital memory in performing the conversion." (Dowdy 082 at Abstract.) "The camera head and endoscope are typically detachable as a unit from the control unit so that a variety of camera heads can be used with a single control unit. This offers a number of advantages. For example, if a first camera head fails, the control unit can be operated with another camera head while

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		the first camera head is being serviced. Also, different types of camera heads, each of which may be most useful for certain procedures, can be used with a single control unit so as to avoid the expense of purchasing and maintaining multiple control units." (Dowdy 082 at 1:25-34 (Background of the Invention).) "In one general aspect, this invention features an apparatus for providing electrical signals that represent an optical image to a processor for conversion to video signals suitable for display on a display device. The apparatus includes a device for insertion into a region to be viewed for developing an optical image of the region, an imager for generating electrical signals that represent the optical image, and a digital memory for storing information about the imager. The device is adapted to be connected to the processor so that the processor can receive the electrical signals from the imager and obtain information from the digital memory. The processor uses the information from the digital memory in performing the conversion." (Dowdy 082 at 1:38-50 (Summary of the Invention).) "The digital memory stores information about the configuration of the imager. This information can include the location of the imager relative to the device. For example, the information identifies whether the imager is located at the distal end or the proximal end of the device. The imager is a charge coupled device. The information identifies an optical format size of the charge coupled device." (Dowdy 082 at 1:53-59.)

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		"The digital memory also stores information about variations in performance characteristics of the imager relative to nominal performance characteristics. When the apparatus includes optics, the information in the digital memory accounts for variations in performance characteristics of the optics relative to nominal performance characteristics. Similarly, when the imager includes a charge coupled device or a cable for connection to the processor, the information accounts for variations in performance characteristics of the charge coupled device or the cable relative to nominal performance characteristics. The information also identifies variations in luminance and color reproduction by the imager." (Dowdy 082 at 1:60-2:5 (Summary of the Invention).) "When the apparatus is designed for application to particular regions, the information identifies characteristics of the region to be viewed by the imager. This allows the processor to optimize the conversion for parameters that are desirable in a particular application." (Dowdy 082 at 2:6-10.) "In one embodiment, the digital memory is a non-volatile storage device, and can be implemented using an EEPROM." (Dowdy 082 at 2:16-17.) "When the information stored in the digital memory identifies the configuration of the device, the processor modifies the conversion based on the configuration. This allows the processor to automatically optimize the

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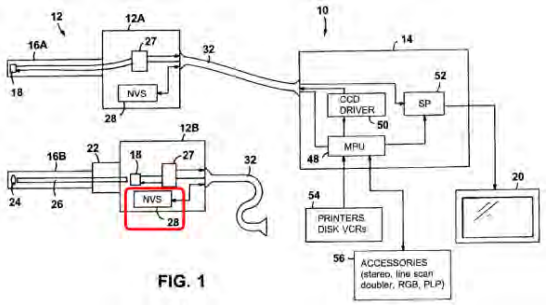
Claims	**Asaida 782**	**in combination with one or more of the following references**
		conversion for different configurations of the device." (Dowdy 082 at 2:34-38.) "Referring also to FIG. 2, to enable different types of camera heads 12 to be used with camera processor 14 without impacting the quality of the video image displayed on video monitor 20, each camera head 12A, 12B (referred to generally with reference numeral 12) includes a non-volatile storage device ("NVS") 28 that stores information identifying the configuration 30 of the particular camera head 12A, 12B. Camera processor 14 uses the information stored in NVS 28 to modify processing of the electrical signals produced by camera head 12, and thereby accounts for the properties of the configuration 30 to which camera head 12 belongs. In a preferred embodiment, NVS 28 is implemented as an electrically erasable programmable read only memory ("EEPROM"). One such EEPROM is an eight pin, 256 byte storage capacity memory available from the Xicor Corp. as model number 24XC02." (Dowdy 082 at 3:62-4:10.)  FIG. 1

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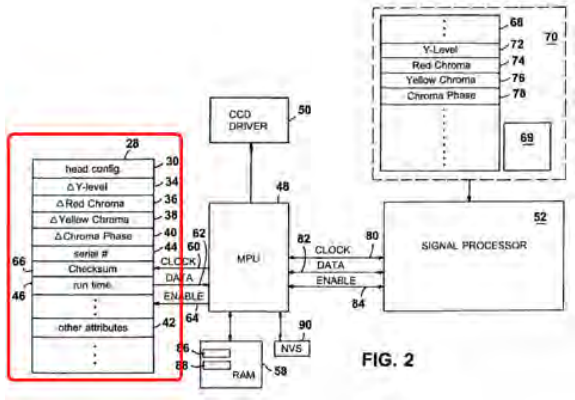
		Dowdy 082 (Figure 1)  FIG. 2 Dowdy 082 (Figure 2) "In addition to variations caused by the configuration of camera head 12, the electrical signals produced by camera head 12 can also vary, because performance characteristics of camera heads 12 tend to vary from device to device. These variations, which are caused primarily by differences in optics, CCDs 18, and cables 32 that are attached to camera heads 12 and connect camera heads 12 to camera processor 14, can adversely affect the ability of a camera head 12 to produce electrical signals that result in an optimal video image. Thus, to further ensure consistent performance when different camera heads 12 are used, NVS 28 also stores information that identifies variations in the performance characteristics of a particular camera head 12 from nominal

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		values." (Dowdy 082 at 4:11-24.) "To enable the video image produced at video monitor 20 to be optimized for certain procedures, the NVS 28 of a camera head 12 designed for those procedures can include information 42 that is used by camera processor 14 to optimize certain signal processing attributes. For example, in a camera head 12 designed for procedures requiring improved edge definition, NVS 28 stores edge enhancement information 42 that replaces nominal edge enhancement values stored within and used by camera processor 14. Similarly, in camera heads 12 designed for procedures in which the white or grey brightness ranges are of particular interest, NVS 28 stores information 42 that modifies, respectively, operation of the so-called "knee circuit" (which implements a nonlinear function for compressing, rather than clipping, the upper level, white, component of the video signal) and the operation of the so-called "gamma circuit" (which implements a nonlinear function for optimizing the median level, grey, component of the video signal) implemented by signal processor 14." (Dowdy 082 at 4:36-54.) "For servicing and other purposes, NVS 28 also stores information that identifies the serial number 44 of camera head 12 and a measure 46, in minutes and hours, of the run time that camera head 12 has experienced." (Dowdy 082 at 4:55-58.) "Referring also to FIG. 3, MPU 48 uses the information

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		stored in NVS 28 to control the operation of CCD driver 50 and signal processing circuitry 52. When the user connects cable 32 of camera head 12 to camera processor 14, and, if necessary, powers up video endoscopy system 10, MPU 48 detects the connection and responds by downloading the information from NVS 28 into a memory 58, such as a RAM, of MPU 48 (step 200). MPU 48 reads the stored information out of NVS 28 through a serial data link in cable 32 that includes a CLOCK line 60 controlled by MPU 48 and a DATA line 62 that is shared by NVS 28 and MPU 48." (Dowdy 082 at 5:9-19.) "Referring to FIG. 4, in a more detailed view, camera head 12 includes CCD 18 (located, as discussed, either in the head or at the tip of the endoscope), NVS 28 and a set of button switches 92 for system control, and camera processor 14 includes a camera controller 94 and a signal processor 96. Cable 32, which connects camera head 12 to camera processor 14, carries drive signals from CCD driver 50 in signal processor 96, electrical signals from CCD 18 to a preamplifier 98 in signal processor 96, data between NVS 28 and MPU 48 in camera controller 94, and signals from button switches 92 to MPU 48." (Dowdy 082 at 6:48-58.)

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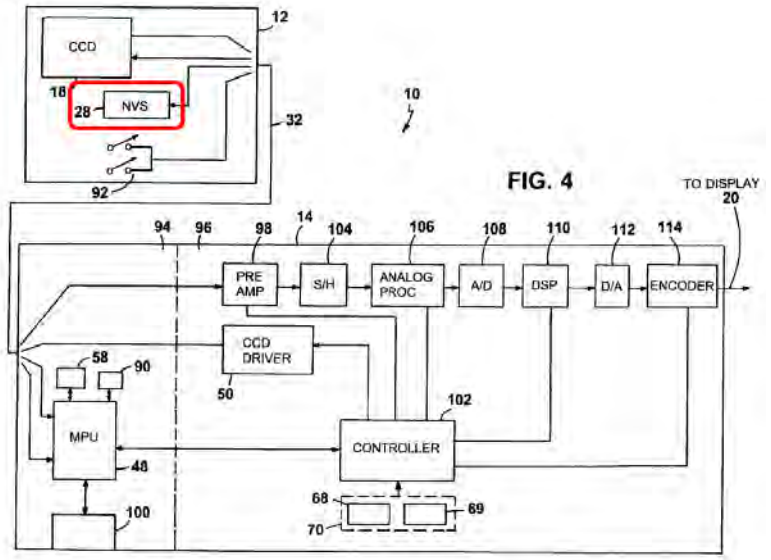
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Dowdy 082 (Figure 4) "MPU 48 controls signal processor 96 in response to signals from button switches 92 and signals from controls in a front panel 100 of camera controller 94. The controls in front panel 100 allow the user of video endoscopy system 10 to configure button switches 92 to perform desired functions. Thus, for example, button switches 92 could be configured to cause signal processor 96 to pause the video image displayed at video monitor 20 (FIG. 1). MPU 48 also displays system parameters at front panel 100, interacts with NVS 28 by downloading information about camera head 12 and updating run time information in NVS 28, updates signal processing

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		parameters in light of the information about camera head 12, and communicates with signal processor 96, all as discussed above." (Dowdy at 6:59-7:5.) "A nonvolatile, programmable memory is incorporated in an endoscope. Endoscope-related data closely relevant to the endoscope, such as, an endoscope model name and the number of power feeds are stored in the nonvolatile memory. The endoscope is connected to an external image processing apparatus, and endoscope-related data is read from the nonvolatile memory. Based on the read endoscope-related data, the use situation of the endoscope is grasped or the endoscope is managed. The number of power feeds is varied depending on the use situation of the endoscope, and written in the nonvolatile memory. Thus, the endoscope-related data is used to maintain the endoscope and reduce a load to be incurred by the external image processing apparatus that is a connected apparatus. Consequently, the endoscope can be managed and maintained easily using a small software system." (Oshima 212 at Abstract.) "[An] object of the present invention is to provide an endoscope system in which endoscope-related data including a use situation of an endoscope can be checked readily." (Oshima 212 at 1:60-62.) "A regulator 19, a programmable nonvolatile memory 20, a CPU 21, a selector (SEL) 22, a supply voltage detector 23, a scope switch 24, and a connector 25 are arranged behind the rear end of the insertion unit 11 of the endoscope 2. The

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		regulator 19 converts a CCD driving voltage fed from a CCD driving power supply 18 incorporated in the image processing apparatus 3A into a desired voltage. The programmable nonvolatile memory 20 in which the endoscope-related data is stored is realized with an EEPROM, a flash ROM, an FRAM, or an MRAM." (Oshima 212 at 6:54-63.) "Especially important data out of endoscope-related data storable in the nonvolatile memory 20 includes, for example, an endoscope model name, the structure of the distal part of an endoscope, a cleaning tube/adaptor name, a CCD model name, a type of optical filter in a CCD, information relating to the channels in an endoscope, information relating to the switches on an endoscope, a version number, and identification data." (Oshima 212 at 29:16-25.)

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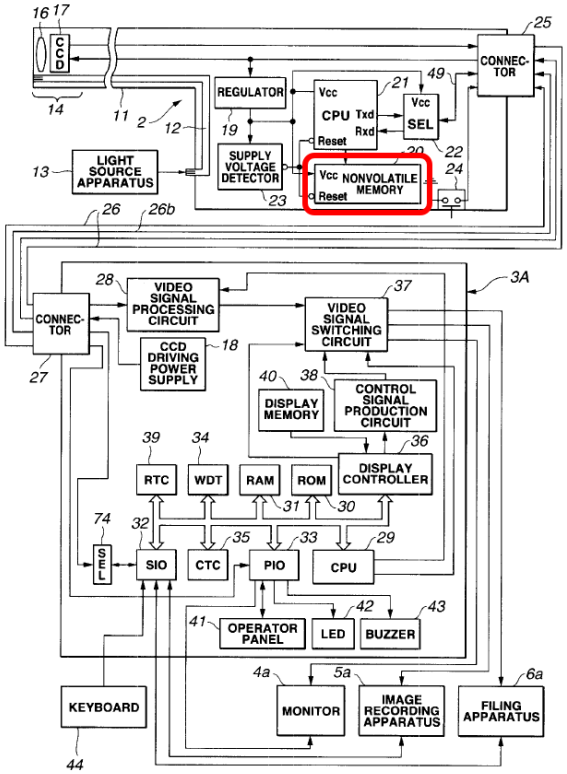
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Oshima 212 (Figure 2) "FIG. 35 describes processing to be performed in the image processing apparatus 3A, which has the ability to communicate with the endoscope 2 and is connected to the endoscope 2, for treating count data contained in data to be stored in the nonvolatile memory 20 in the endoscope 2."

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		(Oshima 212 at 29:59-63.) "The connected apparatus 3A uses connection sensing means (not shown) incorporated in the endoscope and the connected apparatus to judge whether it has been connected to the endoscope 2 (S321). If connection is sensed, identification data or an endoscope model name is read first (S322)." (Oshima 212 at 29:66-30:4.) "From the foregoing description of the prior art, it is clear that the 'bad pixel' data is never transferred to the camera portion, but instead remains in the local controller memory. Accordingly if a camera has been subjected to pixel evaluation for existence of blemishes using a CCU with a blemish compensating capacity as described above, another camera cannot be used in its place with the same CCU unless the CCU blemish compensator is again operated to evaluate the pixels of the new camera. Moreover, assuming that blemish compensation is desired, a camera that has been evaluated by the CCU of Fig. 1 is not interchangeable with another like blemish compensator-equipped CCU unless it is first re-evaluated for blemishes." (Zu 391 at 5-6.) "This non-interchangeability of cameras with a CCU is especially limiting in the case of video endoscopes. During surgery, it may be necessary to employ two or more video endoscopes when only one CCU may be available. With a compensator-equipped CCU as shown in Fig. 1, substitution of one video camera endoscope for another may be frustrated by the need to first evaluate the camera for blemishes and

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		record the 'bad pixels' in the CCU's digital memory so that compensation may be accomplished when video information is acquired by the endoscope's camera." (Zu 391 at 6.) "The object of this invention is to facilitate use of video cameras having known pixel blemishes with different camera control units." (Zu 391 at 6.) "The present invention comprises incorporating into a CCD-type video camera an electronically programmable non-volatile memory which stores the location of 'bad' pixels and is controlled by a device which is located remotely from the camera in a separate CCU. This arrangement assures that video cameras are interchangeable with CCU's regardless of CCD blemish content." (Zu 391 at 6.) "Fig. 2 illustrates the invention. Except as described hereinafter, the system shown in Fig. 2 incorporates the same elements and the same functions as the system of Fig. 1, and identical elements are identified by the same numerals. In this case, the camera 2 is modified by incorporating therein an electronically programmable non-volatile digital memory 42 which is coupled to camera connector 14 via a suitable bus 44." (Zu 391 at 7.)

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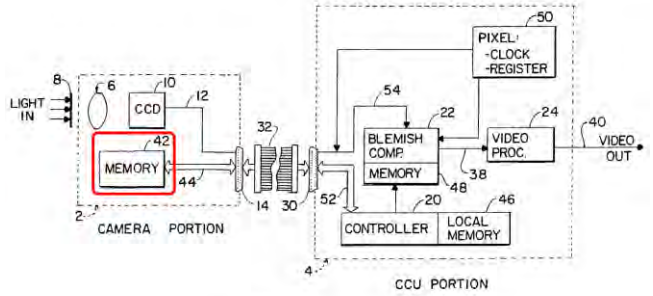
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 FIG. 2 Zu 391 (Figure 2) "In the operational mode, the data in memory 42 is transferred to memories 46 and 48 whenever the unit is energized. The blemish compensation operation is then performed by the blemish compensator 22 using pixel address data downloaded from camera memory 42. The pixel address data is downloaded from camera memory 42 to blemish compensator memory 48 by the controller 20 via the buses 44 and 52." (Zu 391 at 8.) "When the operational mode is initiated with the camera coupled to a CCU 4 as described, the controller 22 downloads the pixel address data from the camera's memory 42 to the protected local memory 46 of the controller 20. Subsequently that data is loaded into the volatile memory 48 of the blemish compensator 22. Typically this data transfer from camera memory 42 t the local memory 46 of the controller occurs after a forced rest imposed by controller 20,

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		which clears, resets, and reloads all non-protected CCU memory." (Zu 391 at 9.)
said camera control unit having at least one digital serial receiver and	"The camera control unit CCU, constituting part of the video camera according to the present invention, is provided with a serial input/output port 40, as shown in FIG. 3, which is connected to the serial input/output port 10 of the camera head unit by an optical fiber cable, not shown, constituting transmission means." (Asaida 782 at 8:5-10.) To the extent this element is not expressly disclosed, it is inherent in Asaida 782. It would be within the knowledge of one of ordinary skill in the art at the time of the alleged invention that transmitting a serial digital signal over a cable would necessarily require a driver to drive the signal and a receiver to receive the signal. Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005) (citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)). Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	To the extent this element is not expressly disclosed, it is inherent in Endsley 471 by virtue of disclosing and claiming USB as a communications medium. Specifically, section 7.1.2 of the USB Specification Revision 1.0 is directed to "Receiver Characteristics": "A differential input receiver must be used to accept the USB data signal. The receiver must feature an input sensitivity of at least 200 mV when both differential data inputs are in the range of at least 0.8 V to 2.5 V with respect to its local ground reference. This is called the common mode input voltage range. Proper data reception is also required when the differential data lines are outside the common mode range, as shown in Figure 7-4. The receiver must tolerate static input voltages between -0.5 V to 3.8 V with respect to its local ground reference without damage. In addition to the differential receiver, there must be a single-ended receiver for each of the two data lines. The receivers must have a switching threshold between 0.8 V and 2.0 V (TTL inputs). It is recommended that the single-ended receiver have some hysteresis to reduce its sensitivity to noise." (USB Spec. Rev. 1.0 at 113.)

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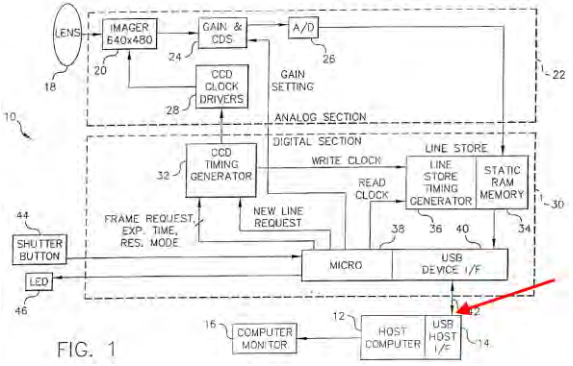
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Endsley 471 (Figure 1) "Reference is now made to FIG. 4, which is an schematic block diagram of the miniature endoscope according to a preferred embodiment of the present invention. Parts that are identical to those shown above are given the same reference numerals and are not referred to again except as necessary for an understanding of the present embodiment. Optical assembly 48 receives light, indicated by arrows 60, from an object being viewed. The light is processed by optical assembly 48, as will be explained below, to reach image sensor 46 were it is converted from photons into electrical signals. The electrical signals are digitized and passed to a transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Adler 940 at 10:7-19 (emphasis added).) If the endoscope uses an LVDS transmitter to drive the data

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		through communication link 20 to the processing device 30, the processing device 30 must necessarily receive the data with a digital serial receiver. ***Alternatively***, this limitation is met if USB is used, rather than LVDS, as a communications medium between the endoscope 10 and processing device 30 as contemplated by the following disclosure. "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope. The skilled person will appreciate that the wire connection 20 may be an optical connection or may instead use RF or a like means of wireless communication. The miniature endoscopic front-end 10 may be designed for connection to any standard PC input (the USB input for example)." (Adler 940 at 9:24-38 (emphasis added).) A receiver would necessarily be required to receive a USB signal over wire connection 20. To the extent this element is not expressly disclosed, it is inherent in Adler 940.

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		Specifically, section 7.1.2 of the USB Specification Revision 1.0 is directed to "Receiver Characteristics": "A differential input receiver must be used to accept the USB data signal. The receiver must feature an input sensitivity of at least 200 mV when both differential data inputs are in the range of at least 0.8 V to 2.5 V with respect to its local ground reference. This is called the common mode input voltage range. Proper data reception is also required when the differential data lines are outside the common mode range, as shown in Figure 7-4. The receiver must tolerate static input voltages between -0.5 V to 3.8 V with respect to its local ground reference without damage. In addition to the differential receiver, there must be a single-ended receiver for each of the two data lines. The receivers must have a switching threshold between 0.8 V and 2.0 V (TTL inputs). It is recommended that the single-ended receiver have some hysteresis to reduce its sensitivity to noise." (USB Spec. Rev. 1.0 at 113.) "Figure 1 shows a typical connection with LVDS drivers and receivers."

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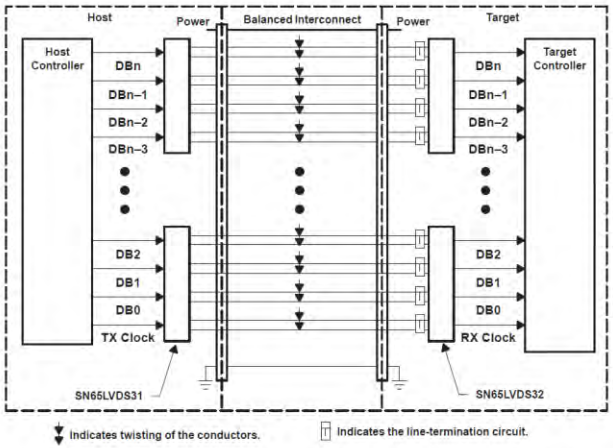
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Figure 1. Typical Connection With LVDS Drivers and Receivers <u>TI LVDS (Figure 1)</u> "The recommended voltage applied to the receiver is between ground and 2.4 V with a common mode range of 0.2 V to 2.2 V. The receiver has a sensitivity level of ±100 mV to correctly assume the intended binary state (see Figure 2). The LVDS interconnecting media must be matched with the 100-Ω termination resistor located at the inputs of the receiver." (TI LVDS at 4.) "There are two configurations that are used in LVDS applications, point-to-point and multi-drop. The Virtex-E family supports both LVDS configurations. **Point-to-Point**

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		In point-to-point configuration, there is one transmitter and one receiver. The LVDS driver is a current source that drives a differential pair of lines. The typical current drive is 3.5 mA. The receiver has high DC impedance. The majority of the driver current flows across the termination resistor generating about 350 mV at the receiver inputs (Figure 1). **Multi-Drop** A multi-drop LVDS configuration has one transmitter and multiple receivers. The differential termination resistor is placed close to the last receiver (Figure 3)." (Virtex-E LVDS at 2.) Among the many applications that LVDS is suited for are "digital cameras" and "multimedia peripherals." (Virtex-E LVDS at 2-3.) "Figure 1 shows the schematic of a standard LVDS driver driving the Virtex-E receiver. An LVDS driver drives the two 50 W transmission lines into a Virtex-E LVDS receiver. The two 50 W single-ended transmission lines can be micro-strip, strip-line, a 100 W differential twisted pair, or a similar balanced differential transmission line." (Virtex-E LVDS at 3.)

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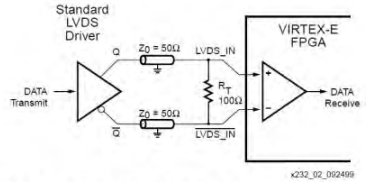
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 **Figure 1: A Standard LVDS Driver Driving a Virtex-E LVDS Receiver** Virtex-E LVDS (Figure 1) "As may be seen, the circuit of FIG. 4 employs a plurality of LVDS circuits 11. Each circuit 11 includes a respective driver 54 and a respective receiver 56. Each driver 54 receives a respective input signal Din0, Din1 . . . Dinn, which are digital logic levels of, for example, 3.3 volts for logic "1" and zero volts for logic "0". Changes in state in these signals are transmitted over the differential lines to the respective receivers 56. Each receiver 56 generates a respective output signal Dout0, Dout1, . . . Doutn, which are at the several hundred millivolt level." (Chung 290 at 2:27-36.)

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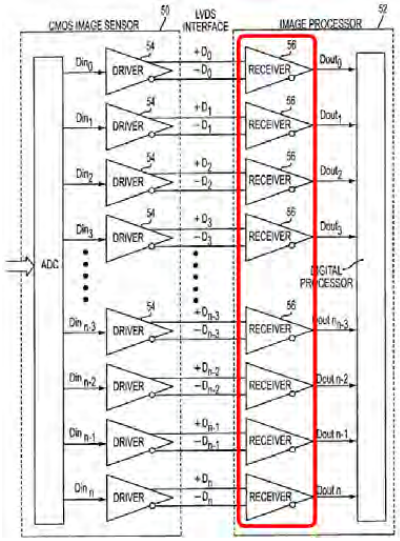
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Chung 290 (Figure 4)
is controlled based at least in part upon said timing signal particular to said camera head.	"[W]ith the present video camera unit, the two-line-concurrent three-color imaging output signals S_{RO}, S_{RE}, S_{GO}, S_{GE}, S_{BO} and S_{BE}, obtained by the solid-state image sensors 2R, 2G, and 2B, are changed by the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE into two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}. The two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, are converted by the P/S converter 7 into serial data as the camera output data $HEAD_{OUT}$, which are serially outputted at the serial input/output port 10 by means of the encoder/decoder 9." (Asaida 782 at 5:50-61.) "[T]he synchronizing circuit block 19 is supplied with a reference	"In FIG. 1 and FIG. 2, the circuit configuration of an electronic endoscope according to the embodiment is shown. In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having a number of scanning lines or the like suitable for the scanning line of the NTSC system, and to this CCD 1, a timing generator 16 is connected, and to this timing generator 16, an NTSC crystal oscillator 17, a PAL crystal oscillator 18, and a switching device 19 are provided. Furthermore, a first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU 20, either of the oscillators 17, 18 is selected." (Okada 852 at

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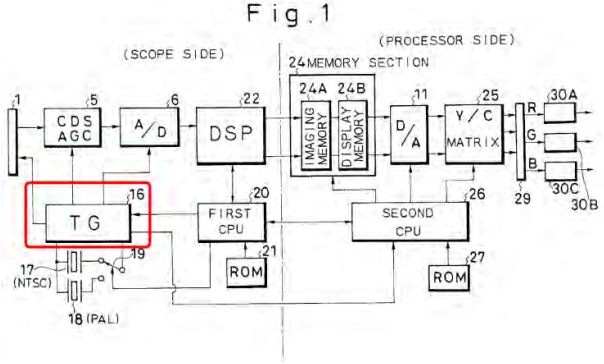
	synchronizing signal $GENLOCK_{REF}$ for generator locking through synchronizing input terminal 27, while the control circuit block 20 is supplied with a control signal CTL through a control input terminal 28." (Asaida 782 at 7:16-21.) "The encoder/decoder 9 encodes the serial data supplied from P/S converters 7 and 31 and serially transmits the encoded serial data via the serial input/output port 10 to a camera control unit CCU described below, while also decoding various serial data transmitted from the camera control unit CCU to the serial input/output port 10, such as return video signals D_{RET}, prompter signals D_{PROMPT}, output signals CCU_{OUT} from the camera control unit CCU or control data D_{CTL}." (Asaida 782 at 7:35-43.) Thus, encoder/decoder 9 transmits either a separate timing signal or a timing signal embedded in the serial data signal received from P/S converter 7 (which originated from image sensors 2R, 2G, and 2B) and sent to the CCU through input/output port 10. The CCU is controlled based at least in part upon the timing signal.	4:4-15.) Fig. 1  Okada 852 (Figure 1) "A first example is configured like the above, and in the example, each television system can be selected by selective switches arranged at the processor or the like, and the state of selection of the switches can be grasped by the second CPU 26. Then, this second CPU 26 reads out the setting data of the selected system from the ROM 27 to set the processing contents of each circuit by this setting data. At the same time, the information of the selected system is also transmitted to the first CPU 20 on the scope side from this second CPU 26, and on this scope side, the selected setting data is read out from the ROM 21 by the first CPU 20 to set the processing contents of each circuit, and further, either of the above oscillators 17, 18 is selected and set." (Okada 852 at 4:58-5:3.)

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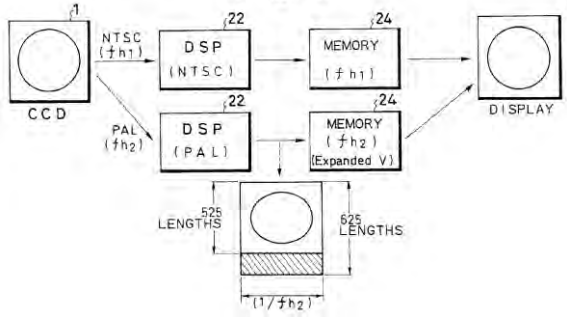
Claims	**Asaida 782**	**in combination with one or more of the following references**
		"That is, if the NTSC system is selected, the NTSC system oscillator 17 is connected to the timing generator 16 by the switching circuit 19. In this timing generator 16, the oscillating signal with, for example, a frequency of 14.32 MHz generated in the oscillator 17 is divided to form the horizontal synchronization signal with a frequency of 15.734 kHz (fh1) and the vertical synchronization signal with a frequency of 59.94 Hz, and the driving pulse based on this is given to the CCD 1. Then, the picture signal extracted from this CCD 1 is subjected to the digital conversion after passing through the AGC circuit 5 for performing the correlative double sampling and the amplification processing, and as shown in FIG. 2, this digital picture signal is subjected to a specified processing by the DSP circuit 22, and it is supplied to the memory section 24 on the processor side." (Okada 852 at 5:4-20.) Fig. 2  Okada 852 (Figure 2)

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		"In this memory section 24, the picture data is written in the imaging memory 24A in the timing of the synchronization signal formed in the timing generator 16, and after that, this picture data is read out in the same timing to be stored in the display memory 24B (as the data corresponding to the number of scanning lines of 525). The data of this display memory 24 is converted into the signals of R, G, and B from the brightness signal and the color difference signal in the Y/C matrix circuit 25 after being converted to the analog signal in the D/A converter 11. Then, each of these signals of R, G, and B is outputted to a monitor of the NTSC system through the isolation device 29 and the buffers 30 (A to C), and consequently, a picture of the NTSC system is displayed on the monitor." (Okada 852 at 5:21-35 (emphasis added).) Thus, the CCU is controlled at least in part based upon said timing signal. "The output of the line store memory 34 is connected to the host computer 12 via the USB device interface 40, which operates at a maximum data rate of 12M bits/sec." (Endsley 471 at 3:37-39.) "[T]he present invention includes a novel way of 'line throttle clocking' the image sensor 20 by varying a line blanking interval 68 from line to line, as shown in FIG. 5, so as to transfer lines of data from the CCD image sensor 20 into the line store memory 34 at the appropriate time." (Endsley 471 at 4:54-59.) "FIG.5 shows that, once the image data is transferred by the readout pulse 60 to the light-protected vertical registers 50,

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		the line clocking is 'throttled' to accommodate the storage capacity of the line store memory 34. The line store memory 34 is capable of storing a small number of lines of data and provides block transfer capability at low cost. Whenever the line store memory 34 has sufficient room to accommodate a new line of image data, the timing generator 32 creates the vertical and horizontal timing pulses 62 and 64 needed to read out the next line from the image sensor, as shown in FIG. 5, and then returns to a wait state until sufficient data is transferred from the line store memory 34 to the computer 12 so as to provide room for the next line. Since the waiting period (equal to the line blanking time) depends on the USB bus traffic, the line readout times and frame readout times are variable, rather than fixed, as in prior art cameras." (Endsley 471 at 4:60-5:9.) The USB Device 40 transmits either a separate timing signal (*see, e.g.*, Section 5.10.2 of USB Spec. Rev. 1.0) or a timing signal embedded in the serial data signal sent to the CCU. The CCU is controlled based at least in part upon the timing signal.
2. The video imaging system according to claim 1 wherein said camera head	*See* Claim 1. The analysis of Claim 1 is incorporated by reference in its entirety. "The multiplexor 18 is supplied with control data D_{CTL} from a synchronizing circuit block 19 and a control circuit block 20, while being supplied with voice data D_{MIC}, from a microphone signal inputted from a microphone input terminal 21 by means of a selector	

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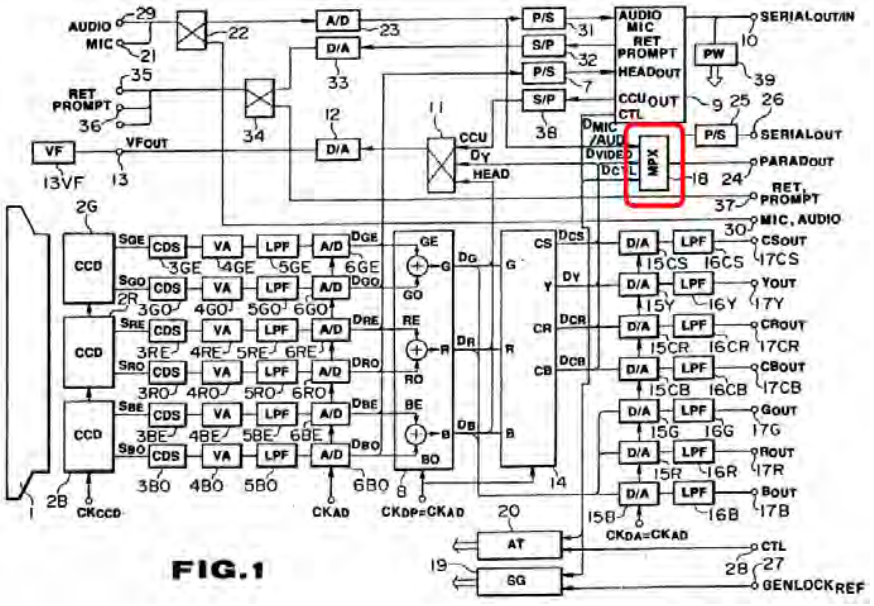
Claims	**Asaida 782**	**in combination with one or more of the following references**
further comprises a multiplexer, for generating a multiplexed signal, which includes the digital image signal and control signals.	22 and digitized by an A/D converter 23 into audio data $D_{MIC/AUDIO}$. The multiplexor 18 adds the signals D_{CTL} and $D_{MIC/AUDIO}$ to a digital video signal D_{VIDEO} composed of the digital component Video signals D_Y, D_{CR} and D_{CB} or the digital composite video signal D_{CS} supplied from the encoder 14. Output data D_{MPX} from the multiplexor 18, that is, the digital video signal D_{VIDEO} added to the control data D_{CTL} and the audio data $D_{MIC/AUDIO}$, are outputted in parallel at a parallel output port 24, while being converted by P/S converter 25 from parallel data into serial data which are serially outputted at a serial output port 26." (Asaida 782 at 6:67-7:15.)  FIG.1 Asaida 782 (Figure 1)	

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Claims	**Asaida 782**	**in combination with one or more of the following references**
3. The video imaging system according to claim 1 wherein said camera head utilizes at least one digital serial receiver.	*See* Claim 1. The analysis of Claim 1 is incorporated by reference in its entirety. "[I]n the present camera control unit CCU, the two-line-concurrent digital three color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, and obtained by the S/P converter 42, are processed by interlacing by the signal processing section 44 either directly or after image processing by the image processing section 43, and the resulting interlaced digital three-color signals D_R, D_G and D_G are serially outputted as the CCU-outputted video data CCU_{OUT} from the serial input/output port 40 over the optical fiber cable to the camera head unit. In the camera head unit, the image represented by the CCU-outputted video data CCU_{OUT}, serially transmitted from the camera control unit CCU to the serial input/output port 10 over the optical fiber cable, is displayed on the view finder 13VF." (Asaida 782 at 8:64-9:10.) To the extent this element is not expressly disclosed, it is inherent in Asaida 782. It would be within the knowledge of one of ordinary skill in the art at the time of the alleged invention that transmitting a serial digital signal over a cable would necessarily require a driver to drive the signal and a receiver to receive the signal. Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005) (citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir.	To the extent this element is not expressly disclosed, it is inherent in Endsley 471 by virtue of disclosing and claiming USB as a communications medium. Specifically, section 7.1.2 of the USB Specification Revision 1.0 is directed to "Receiver Characteristics": "A differential input receiver must be used to accept the USB data signal. The receiver must feature an input sensitivity of at least 200 mV when both differential data inputs are in the range of at least 0.8 V to 2.5 V with respect to its local ground reference. This is called the common mode input voltage range. Proper data reception is also required when the differential data lines are outside the common mode range, as shown in Figure 7-4. The receiver must tolerate static input voltages between -0.5 V to 3.8 V with respect to its local ground reference without damage. In addition to the differential receiver, there must be a single-ended receiver for each of the two data lines. The receivers must have a switching threshold between 0.8 V and 2.0 V (TTL inputs). It is recommended that the single-ended receiver have some hysteresis to reduce its sensitivity to noise." (USB Spec. Rev. 1.0 at 113.)

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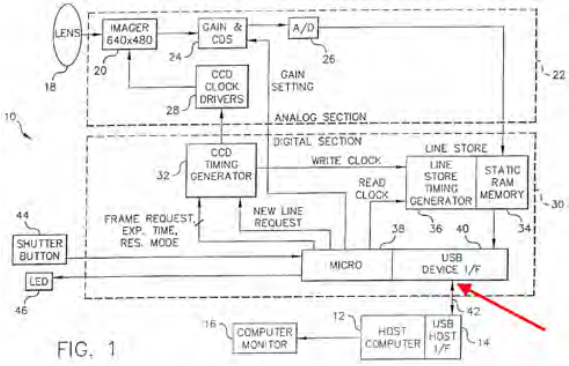
Claims	**Asaida 782**	**in combination with one or more of the following references**
	2000)). Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	 FIG. 1 Endsley 471 (Figure 1) "Operating power for the endoscope 40 is preferably provided, through adapter 44, to the voltage regulator 56. Control of the front-end is preferably carried out by the processor device 30 as discussed above. Control data from the processing device 30 is preferably received at the endoscope 40 by a receiving device 64, which may typically be an LVDS receiver. Hard wired logic 66 preferably serves as an interface to convert the incoming control data into signals for controlling both the sensor 46 and the light source 50." (Adler 940 at 10:20-29.)

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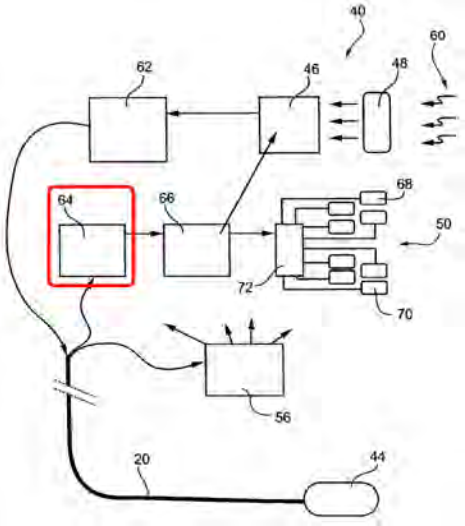
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Adler 940 (Figure 4) In a system that supports bidirectional serial communication, the camera head would necessarily utilize at least on digital serial receiver. "Figure 1 shows a typical connection with LVDS drivers and receivers."

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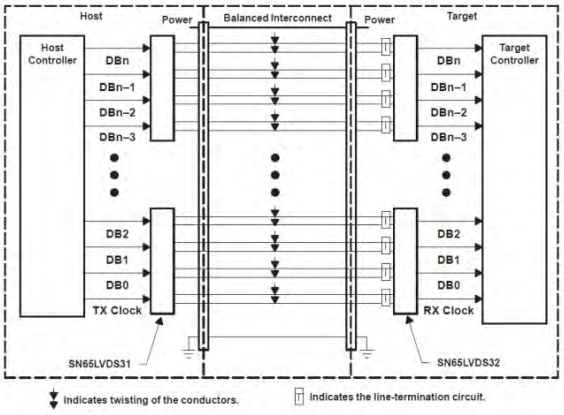
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Figure 1. Typical Connection With LVDS Drivers and Receivers TI LVDS (Figure 1) "The recommended voltage applied to the receiver is between ground and 2.4 V with a common mode range of 0.2 V to 2.2 V. The receiver has a sensitivity level of ±100 mV to correctly assume the intended binary state (see Figure 2). The LVDS interconnecting media must be matched with the 100-Ω termination resistor located at the inputs of the receiver." (TI LVDS at 4.) In a system that supports bidirectional serial communication, the camera head would necessarily utilize at least on digital serial receiver. "There are two configurations that are used in LVDS applications, point-to-point and multi-drop. The Virtex-E

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		family supports both LVDS configurations. **Point-to-Point** In point-to-point configuration, there is one transmitter and one receiver. The LVDS driver is a current source that drives a differential pair of lines. The typical current drive is 3.5 mA. The receiver has high DC impedance. The majority of the driver current flows across the termination resistor generating about 350 mV at the receiver inputs (Figure 1). **Multi-Drop** A multi-drop LVDS configuration has one transmitter and multiple receivers. The differential termination resistor is placed close to the last receiver (Figure 3)." (Virtex-E LVDS at 2.) Among the many applications that LVDS is suited for are "digital cameras" and "multimedia peripherals." (Virtex-E LVDS at 2-3.) "Figure 1 shows the schematic of a standard LVDS driver driving the Virtex-E receiver. An LVDS driver drives the two 50 W transmission lines into a Virtex-E LVDS receiver. The two 50 W single-ended transmission lines can be micro-strip, strip-line, a 100 W differential twisted pair, or a similar balanced differential transmission line." (Virtex-E LVDS at 3.)

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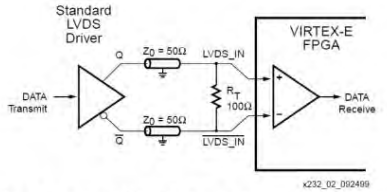
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 **Figure 1: A Standard LVDS Driver Driving a Virtex-E LVDS Receiver** <u>Virtex-E LVDS (Figure 1)</u> It would have been obvious to one of ordinary skill in the art to add include a digital serial receiver as disclosed by Chung in the camera head. "As may be seen, the circuit of FIG. 4 employs a plurality of LVDS circuits 11. Each circuit 11 includes a respective driver 54 and a respective receiver 56. Each driver 54 receives a respective input signal Din0, Din1 . . . Dinn, which are digital logic levels of, for example, 3.3 volts for logic "1" and zero volts for logic "0". Changes in state in these signals are transmitted over the differential lines to the respective receivers 56. Each receiver 56 generates a respective output signal Dout0, Dout1, . . . Doutn, which are at the several hundred millivolt level." (Chung 290 at 2:27-36.)

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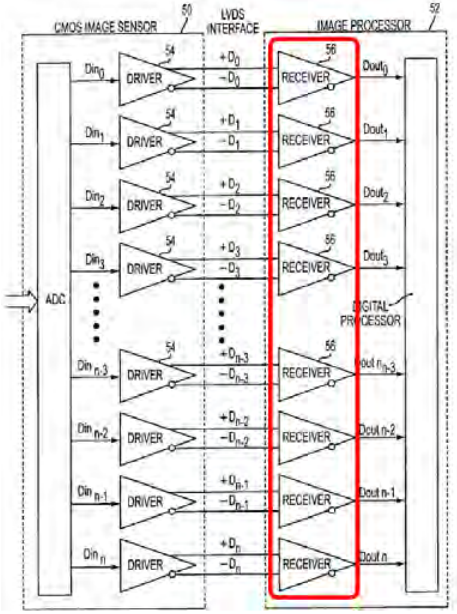
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Chung 290 (Figure 4)
4. Said camera head according to claim 3 wherein the at least one digital serial receiver utilizes Low-	*See* Claim 3. The analysis of Claim 3 is incorporated by reference in its entirety. Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005) (citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)).	"Operating power for the endoscope 40 is preferably provided, through adapter 44, to the voltage regulator 56. Control of the front-end is preferably carried out by the processor device 30 as discussed above. Control data from the processing device 30 is preferably received at the endoscope 40 by a receiving device 64, which may typically be an LVDS receiver. Hard wired logic 66 preferably serves as an interface to convert the incoming control data into signals for controlling both the sensor 46 and the light source 50." (Adler 940 at 10:20-29.)

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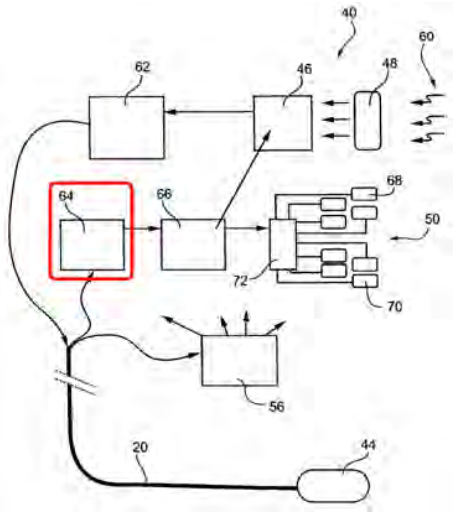
Claims	**Asaida 782**	**in combination with one or more of the following references**
Voltage Differential Signals.	Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	 Adler 940 (Figure 4) "Figure 1 shows a typical connection with LVDS drivers and receivers."

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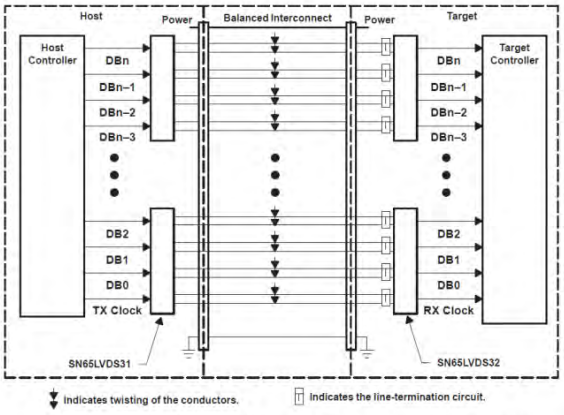
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Figure 1. Typical Connection With LVDS Drivers and Receivers TI LVDS (Figure 1) "The recommended voltage applied to the receiver is between ground and 2.4 V with a common mode range of 0.2 V to 2.2 V. The receiver has a sensitivity level of ±100 mV to correctly assume the intended binary state (see Figure 2). The LVDS interconnecting media must be matched with the 100-Ω termination resistor located at the inputs of the receiver." (TI LVDS at 4.) "Figure 1 shows the schematic of a standard LVDS driver driving the Virtex-E receiver. An LVDS driver drives the two 50 W transmission lines into a Virtex-E LVDS receiver. The two 50 W single-ended transmission lines can be micro-strip, strip-line, a 100 W differential twisted pair, or a similar balanced differential transmission line." (Virtex-E LVDS at

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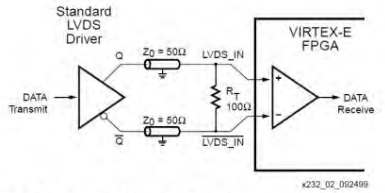
Claims	**Asaida 782**	**in combination with one or more of the following references**
		3.)  **Figure 1: A Standard LVDS Driver Driving a Virtex-E LVDS Receiver** <u>Virtex-E LVDS (Figure 1)</u> "As may be seen, the circuit of FIG. 4 employs a plurality of LVDS circuits 11. Each circuit 11 includes a respective driver 54 and a respective receiver 56. Each driver 54 receives a respective input signal Din0, Din1 . . . Dinn, which are digital logic levels of, for example, 3.3 volts for logic "1" and zero volts for logic "0". Changes in state in these signals are transmitted over the differential lines to the respective receivers 56. Each receiver 56 generates a respective output signal Dout0, Dout1, . . . Doutn, which are at the several hundred millivolt level." (Chung 290 at 2:27-36.)

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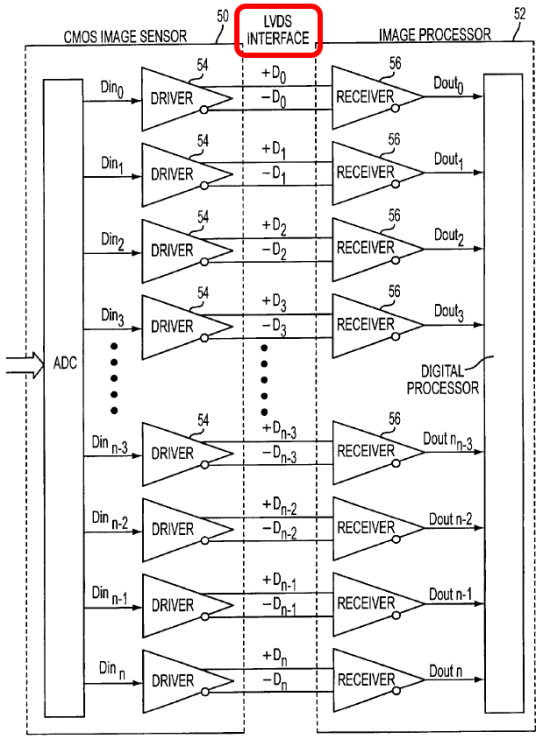
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Chung 290 (Figure 4)
5. Said camera head according to claim 1 wherein the at least one	*See* Claim 1. The analysis of Claim 1 is incorporated by reference in its entirety. Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her	"Reference is now made to FIG. 4, which is an schematic block diagram of the miniature endoscope according to a preferred embodiment of the present invention. Parts that are identical to those shown above are given the same reference numerals and are not referred to again except as necessary for an understanding of the present embodiment. Optical

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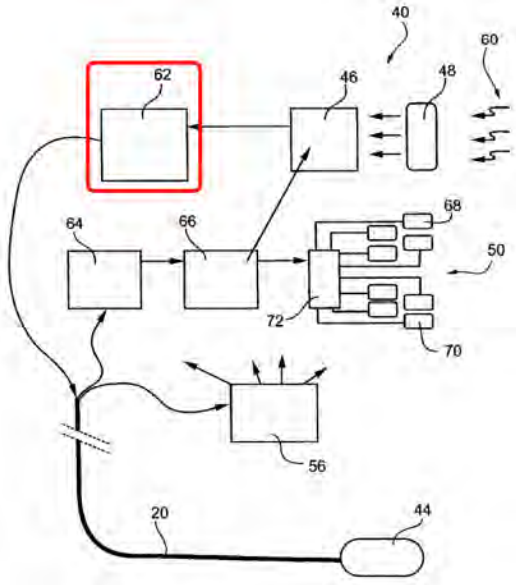
Claims	**Asaida 782**	**in combination with one or more of the following references**
digital serial driver utilizes Low-Voltage Differential Signals.	own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005) (citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)). Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	assembly 48 receives light, indicated by arrows 60, from an object being viewed. The light is processed by optical assembly 48, as will be explained below, to reach image sensor 46 were it is converted from photons into electrical signals. The electrical signals are digitized and passed to a transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Adler 940 at 10:7-19.)  Adler 940 (Figure 4) "Figure 1 shows a typical connection with LVDS drivers and receivers."

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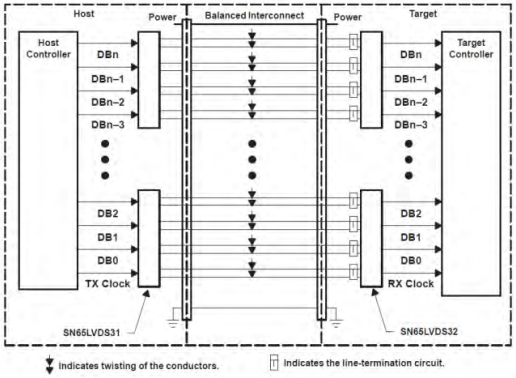
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Figure 1. Typical Connection With LVDS Drivers and Receivers TI LVDS (Figure 1) "The LVDS driver produces a differential voltage across a 100-Ω load in the range of 247 mV to 454 mV with a typical offset voltage of 1.2 V relative to ground (see Figure 2). Most drivers are commonly imple3mented as current-mode devices, which allow frequency to be virtually independent of power consumption. These two characteristics, low voltage swings and constant current, allow LVDS drivers to operate at higher data rates and lower power dissipation." (TI LVDS at 2.) "Figure 1 shows the schematic of a standard LVDS driver driving the Virtex-E receiver. An LVDS driver drives the two 50 W transmission lines into a Virtex-E LVDS receiver. The two 50 W single-ended transmission lines can be micro-strip, strip-line, a 100 W differential twisted pair, or a similar

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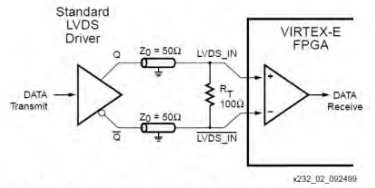
		balanced differential transmission line." (Virtex-E LVDS at 3.)  Figure 1: A Standard LVDS Driver Driving a Virtex-E LVDS Receiver Virtex-E LVDS (Figure 1) "As may be seen, the circuit of FIG. 4 employs a plurality of LVDS circuits 11. Each circuit 11 includes a respective driver 54 and a respective receiver 56. Each driver 54 receives a respective input signal Din0, Din1 . . . Dinn, which are digital logic levels of, for example, 3.3 volts for logic "1" and zero volts for logic "0". Changes in state in these signals are transmitted over the differential lines to the respective receivers 56. Each receiver 56 generates a respective output signal Dout0, Dout1, . . . Doutn, which are at the several hundred millivolt level." (Chung 290 at 2:27-36.)

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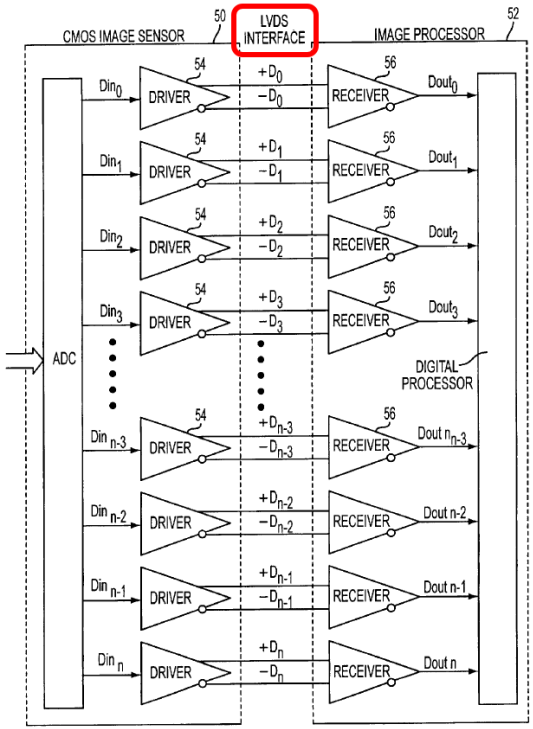
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Chung 290 (Figure 4)
6. The video imaging system according to claim 1 wherein said	*See* Claim 1. The analysis of Claim 1 is incorporated by reference in its entirety. "[I]n the present camera control unit CCU, the two-line-concurrent digital three color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, and obtained by the S/P converter 42, are processed by interlacing by the	To the extent this element is not expressly disclosed, it is inherent in Endsley 471 by virtue of disclosing and claiming USB as a communications medium. Specifically, section 7.1.1 of the USB Specification Revision 1.0 is directed to "USB Driver Characteristics":

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Claims	**Asaida 782**	**in combination with one or more of the following references**
camera control unit utilizes at least one digital serial driver.	signal processing section 44 either directly or after image processing by the image processing section 43, and the resulting interlaced digital three-color signals D_R, D_G and D_G are serially outputted as the CCU-outputted video data CCU_{OUT} from the serial input/output port 40 over the optical fiber cable to the camera head unit. In the camera head unit, the image represented by the CCU-outputted video data CCU_{OUT}, serially transmitted from the camera control unit CCU to the serial input/output port 10 over the optical fiber cable, is displayed on the view finder 13VF." (Asaida 782 at 8:64-9:10.) To the extent this element is not expressly disclosed, it is inherent in Asaida 782. It would be within the knowledge of one of ordinary skill in the art at the time of the alleged invention that transmitting a serial digital signal over a cable would necessarily require a driver to drive the signal and a receiver to receive the signal. Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005) (citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)). Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	"The USB uses a differential output driver to drive the USB data signal onto the USB cable. The static output swing of the driver in its low state must be below the VOL of 0.3 V with a 1.5 kW load to 3.6 V and in its high state must be above the VOH of 2.8 V with a 15 kW load to ground as listed in Table 7-4. The output swings between the differential high and low state must be well balanced to minimize signal skew. Slew rate control on the driver is required to minimize the radiated noise and cross talk. The driver's outputs must support three-state operation to achieve bi-directional half duplex operation. High impedance is also required to isolate the port from downstream devices that are being hot inserted or which are connected but powered down. The driver must tolerate a voltage on the signal pins of -0.5 V to 3.8 V with respect to local ground reference without damage. It must tolerate this voltage for 10.0 μs while the driver is active and driving, and tolerate the condition indefinitely when the driver is in its high impedance state." (USB Spec. Rev. 1.0 at 111-13.)

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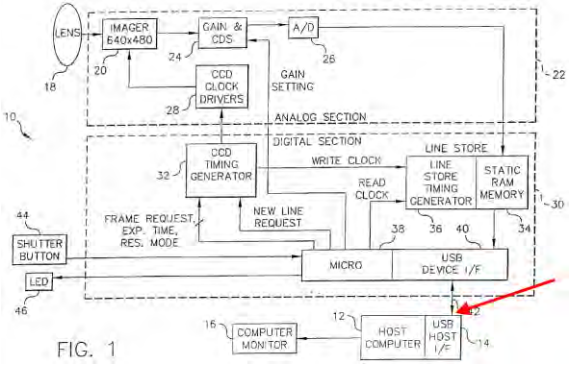
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Endsley 471 (Figure 1) "Operating power for the endoscope 40 is preferably provided, through adapter 44, to the voltage regulator 56. Control of the front-end is preferably carried out by the processor device 30 as discussed above. Control data from the processing device 30 is preferably received at the endoscope 40 by a receiving device 64, which may typically be an LVDS receiver. Hard wired logic 66 preferably serves as an interface to convert the incoming control data into signals for controlling both the sensor 46 and the light source 50." (Adler 940 at 10:20-29 (emphasis added).) If the endoscope uses an LVDS receiver to receive control data from the processing device 30, the processing device 30 must necessarily drive the data to the endoscope using at least one digital serial driver. ***Alternatively***, this limitation is met if USB is used, rather

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		than LVDS, as a communications medium between the endoscope 10 and processing device 30 as contemplated by the following disclosure. "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope. The skilled person will appreciate that the wire connection 20 may be an optical connection or may instead use RF or a like means of wireless communication. The miniature endoscopic front-end 10 may be designed for connection to any standard PC input (the USB input for example)." (Adler 940 at 9:24-38 (emphasis added).) A driver would necessarily be required to drive a USB signal over wire connection 20. To the extent this element is not expressly disclosed, it is inherent in Adler 940. Specifically, section 7.1.1 of the USB Specification Revision 1.0 is directed to "USB Driver Characteristics": "The USB uses a differential output driver to drive the USB data signal onto the USB cable. The static output swing of

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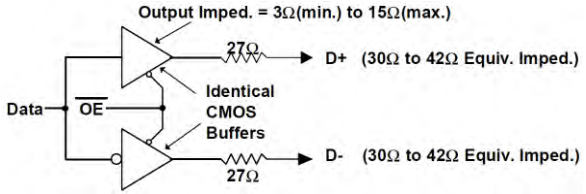
Claims	**Asaida 782**	**in combination with one or more of the following references**
		the driver in its low state must be below the VOL of 0.3 V with a 1.5 kW load to 3.6 V and in its high state must be above the VOH of 2.8 V with a 15 kW load to ground as listed in Table 7-4. The output swings between the differential high and low state must be well balanced to minimize signal skew. Slew rate control on the driver is required to minimize the radiated noise and cross talk. The driver's outputs must support three-state operation to achieve bi-directional half duplex operation. High impedance is also required to isolate the port from downstream devices that are being hot inserted or which are connected but powered down. The driver must tolerate a voltage on the signal pins of -0.5 V to 3.8 V with respect to local ground reference without damage. It must tolerate this voltage for 10.0 µs while the driver is active and driving, and tolerate the condition indefinitely when the driver is in its high impedance state." (USB Spec. Rev. 1.0 at 111-13.)  USB Spec. Rev. 1.0 (Figure 7-1) In a system that supports bidirectional serial communication, the camera control unit would necessarily utilize at least on digital serial driver.

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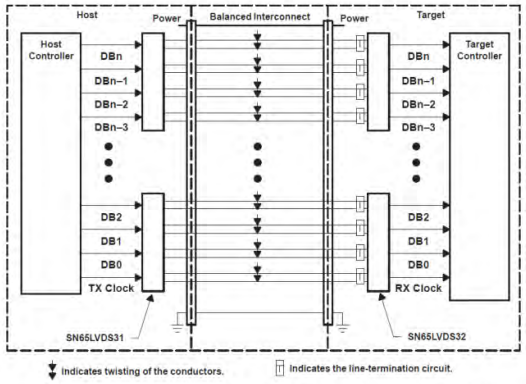
Claims	**Asaida 782**	**in combination with one or more of the following references**
		"Figure 1 shows a typical connection with LVDS drivers and receivers."  Figure 1. Typical Connection With LVDS Drivers and Receivers TI LVDS (Figure 1) "The LVDS driver produces a differential voltage across a 100-Ω load in the range of 247 mV to 454 mV with a typical offset voltage of 1.2 V relative to ground (see Figure 2). Most drivers are commonly imple3mented as current-mode devices, which allow frequency to be virtually independent of power consumption. These two characteristics, low voltage swings and constant current, allow LVDS drivers to operate at higher data rates and lower power dissipation." (TI LVDS at 2.) In a system that supports bidirectional serial communication,

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		the camera control unit would necessarily utilize at least on digital serial driver. "There are two configurations that are used in LVDS applications, point-to-point and multi-drop. The Virtex-E family supports both LVDS configurations. **Point-to-Point** In point-to-point configuration, there is one transmitter and one receiver. The LVDS driver is a current source that drives a differential pair of lines. The typical current drive is 3.5 mA. The receiver has high DC impedance. The majority of the driver current flows across the termination resistor generating about 350 mV at the receiver inputs (Figure 1). **Multi-Drop** A multi-drop LVDS configuration has one transmitter and multiple receivers. The differential termination resistor is placed close to the last receiver (Figure 3)." (Virtex-E LVDS at 2.) Among the many applications that LVDS is suited for are "digital cameras" and "multimedia peripherals." (Virtex-E LVDS at 2-3.) "Figure 1 shows the schematic of a standard LVDS driver driving the Virtex-E receiver. An LVDS driver drives the two 50 W transmission lines into a Virtex-E LVDS receiver. The two 50 W single-ended transmission lines can be micro-strip, strip-line, a 100 W differential twisted pair, or a similar

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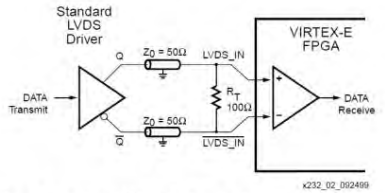
Claims	**Asaida 782**	**in combination with one or more of the following references**
		balanced differential transmission line." (Virtex-E LVDS at 3.)  **Figure 1: A Standard LVDS Driver Driving a Virtex-E LVDS Receiver** Virtex-E LVDS (Figure 1) It would have been obvious to one of ordinary skill in the art to add include a digital serial driver as disclosed by Chung in the camera control unit. "As may be seen, the circuit of FIG. 4 employs a plurality of LVDS circuits 11. Each circuit 11 includes a respective driver 54 and a respective receiver 56. Each driver 54 receives a respective input signal Din0, Din1 . . . Dinn, which are digital logic levels of, for example, 3.3 volts for logic "1" and zero volts for logic "0". Changes in state in these signals are transmitted over the differential lines to the respective receivers 56. Each receiver 56 generates a respective output signal Dout0, Dout1, . . . Doutn, which are at the several hundred millivolt level." (Chung 290 at 2:27-36.)

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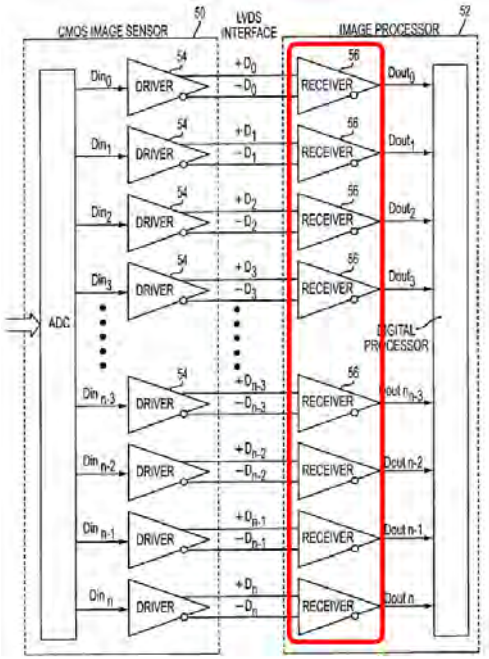
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Chung 290 (Figure 4)
7. Said camera control unit according to claim 6 wherein the at least one digital serial	*See* Claim 6. The analysis of Claim 6 is incorporated by reference in its entirety. Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005)	"Operating power for the endoscope 40 is preferably provided, through adapter 44, to the voltage regulator 56. Control of the front-end is preferably carried out by the processor device 30 as discussed above. Control data from the processing device 30 is preferably received at the endoscope 40 by a receiving device 64, which may typically be an LVDS receiver. Hard wired logic 66 preferably serves as an interface to convert the incoming control data into

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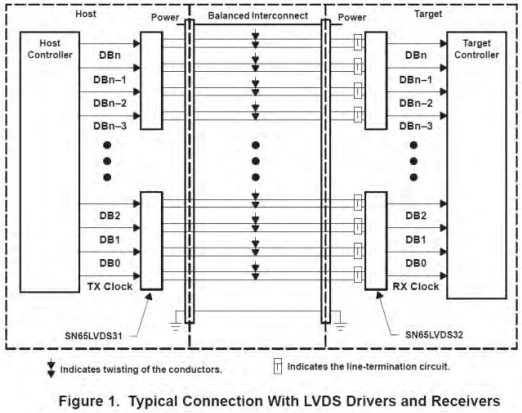
Claims	**Asaida 782**	**in combination with one or more of the following references**
driver utilizes Low-Voltage Differential Signals.	(citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)). Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	signals for controlling both the sensor 46 and the light source 50." (Adler 940 at 10:20-29 (emphasis added).) If the endoscope uses an LVDS receiver to receive control data from the processing device 30, the processing device 30 must necessarily drive the data to the endoscope using at least one digital serial driver that utilizes Low-Voltage Differential Signals. "Figure 1 shows a typical connection with LVDS drivers and receivers."  Figure 1. Typical Connection With LVDS Drivers and Receivers TI LVDS (Figure 1) "The LVDS driver produces a differential voltage across a 100-Ω load in the range of 247 mV to 454 mV with a typical offset voltage of 1.2 V relative to ground (see Figure 2).

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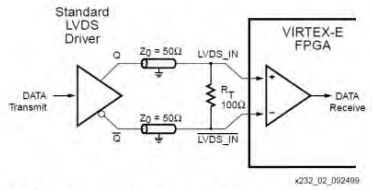
Claims	**Asaida 782**	**in combination with one or more of the following references**
		Most drivers are commonly imple3mented as current-mode devices, which allow frequency to be virtually independent of power consumption. These two characteristics, low voltage swings and constant current, allow LVDS drivers to operate at higher data rates and lower power dissipation." (TI LVDS at 2.) "Figure 1 shows the schematic of a standard LVDS driver driving the Virtex-E receiver. An LVDS driver drives the two 50 W transmission lines into a Virtex-E LVDS receiver. The two 50 W single-ended transmission lines can be micro-strip, strip-line, a 100 W differential twisted pair, or a similar balanced differential transmission line." (Virtex-E LVDS at 3.)  **Figure 1: A Standard LVDS Driver Driving a Virtex-E LVDS Receiver** Virtex-E LVDS (Figure 1) "As may be seen, the circuit of FIG. 4 employs a plurality of LVDS circuits 11. Each circuit 11 includes a respective driver 54 and a respective receiver 56. Each driver 54 receives a respective input signal Din0, Din1 . . . Dinn, which are digital logic levels of, for example, 3.3 volts for

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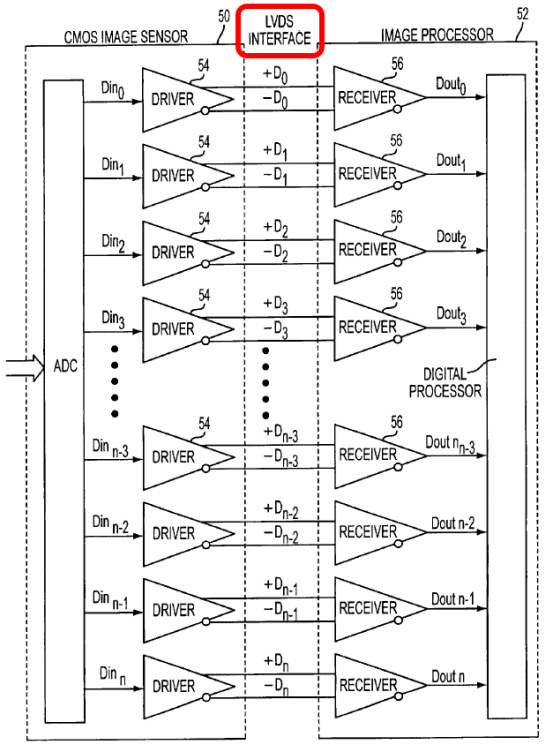
Claims	**Asaida 782**	**in combination with one or more of the following references**
		logic "1" and zero volts for logic "0". Changes in state in these signals are transmitted over the differential lines to the respective receivers 56. Each receiver 56 generates a respective output signal Dout0, Dout1, . . . Doutn, which are at the several hundred millivolt level." (Chung 290 at 2:27-36.)  Chung 290 (Figure 4)

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Claims	**Asaida 782**	**in combination with one or more of the following references**
8. Said camera control unit according to claim 1 wherein the at least one digital serial receiver utilizes Low-Voltage Differential Signals.	*See* Claim 1. The analysis of Claim 1 is incorporated by reference in its entirety. Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005) (citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)). Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	"Reference is now made to FIG. 4, which is an schematic block diagram of the miniature endoscope according to a preferred embodiment of the present invention. Parts that are identical to those shown above are given the same reference numerals and are not referred to again except as necessary for an understanding of the present embodiment. Optical assembly 48 receives light, indicated by arrows 60, from an object being viewed. The light is processed by optical assembly 48, as will be explained below, to reach image sensor 46 were it is converted from photons into electrical signals. The electrical signals are digitized and passed to a transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Adler 940 at 10:7-19.) If the electrical signals are transmitted to the processing device 30 using an LVDS transmitter, the at least one digital serial receiver in the processing device that receives the signals must necessarily utilize Low-Voltage Differential Signals. "Figure 1 shows a typical connection with LVDS drivers and receivers."

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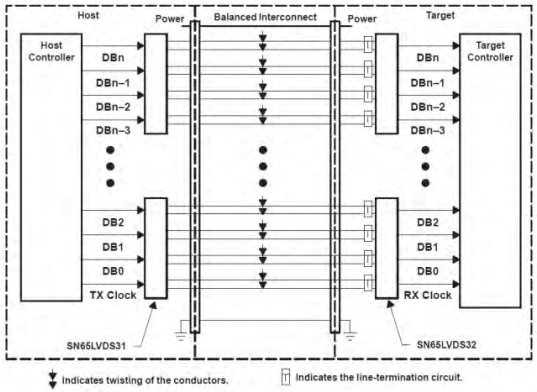
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Figure 1. Typical Connection With LVDS Drivers and Receivers TI LVDS (Figure 1) "The recommended voltage applied to the receiver is between ground and 2.4 V with a common mode range of 0.2 V to 2.2 V. The receiver has a sensitivity level of ±100 mV to correctly assume the intended binary state (see Figure 2). The LVDS interconnecting media must be matched with the 100-Ω termination resistor located at the inputs of the receiver." (TI LVDS at 4.) "Figure 1 shows the schematic of a standard LVDS driver driving the Virtex-E receiver. An LVDS driver drives the two 50 W transmission lines into a Virtex-E LVDS receiver. The two 50 W single-ended transmission lines can be micro-strip, strip-line, a 100 W differential twisted pair, or a similar balanced differential transmission line." (Virtex-E LVDS at 3.)

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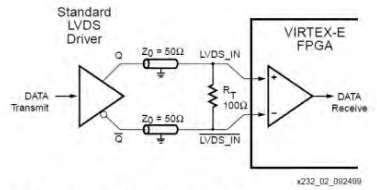
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 **Figure 1: A Standard LVDS Driver Driving a Virtex-E LVDS Receiver** <u>Virtex-E LVDS (Figure 1)</u> "As may be seen, the circuit of FIG. 4 employs a plurality of LVDS circuits 11. Each circuit 11 includes a respective driver 54 and a respective receiver 56. Each driver 54 receives a respective input signal Din0, Din1 . . . Dinn, which are digital logic levels of, for example, 3.3 volts for logic "1" and zero volts for logic "0". Changes in state in these signals are transmitted over the differential lines to the respective receivers 56. Each receiver 56 generates a respective output signal Dout0, Dout1, . . . Doutn, which are at the several hundred millivolt level." (Chung 290 at 2:27-36.)

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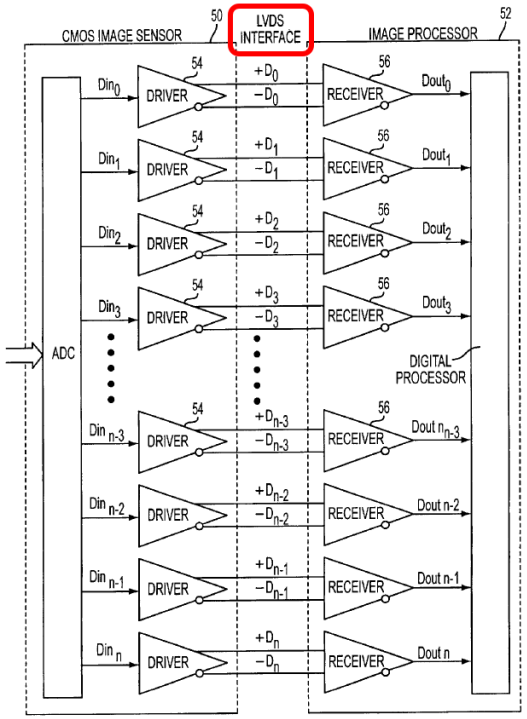
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Chung 290 (Figure 4)
9. A video imaging system comprising:	To the extent the preamble is limiting, Asaida 782 discloses "[a] video imaging system." "This invention relates to a video camera forming digital signals representing an object projected on an imaging device and, more particularly, to a video camera having a signal processing circuit for performing digital signal processing on output signals of the imaging	To the extent the preamble is limiting, Okada 852 discloses "[a] video imaging system." "The present invention relates to an imaging device for an endoscope, and more particularly, it relates to the composition of an endoscope system which can display a picture imaged by using one scope, by either system selected

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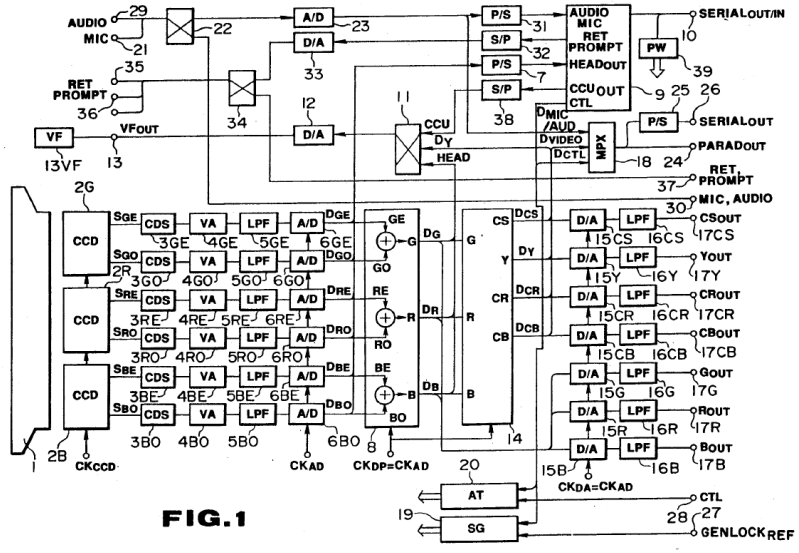
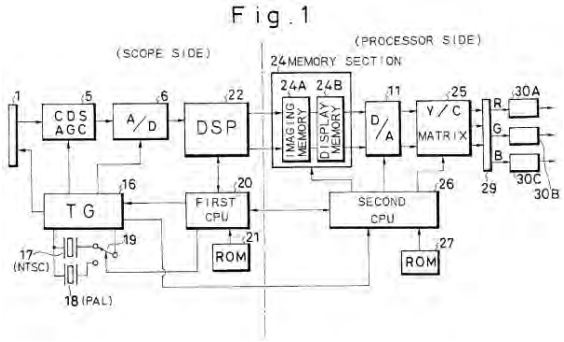
Claims	**Asaida 782**	**in combination with one or more of the following references**
	device." (Asaida 782 at 1:7-12.) "FIG. 1 is a block diagram showing an embodiment of a camera head unit of a video camera according to the present invention." (Asaida 782 at 3:44-46.)  FIG.1 Asaida 782 (Figure 1) "FIG. 3 is a block diagram showing an embodiment of a camera control unit of the video camera shown in FIG. 1." (Asaida 782 at 3:50-52.)	from the NTSC system and the PAL system." (Okada 852 at 1:12-16." "FIG. 1 is a block diagram showing the circuit configuration of an electronic endoscope equipped with both the NTSC system and the PAL system according to an embodiment of the present invention." (Okada 852 at 3:58-61.)  Okada 852 (Figure 1) To the extent the preamble is limiting, Endsley 471 discloses a video imaging system. Specifically, "[a] block diagram of a digital imaging system according to the invention is shown in FIG. 1. The system includes a camera 10 connected to a host computer 12 via a USB (universal serial bus) cable 42 connected to a USB digital host interface 14, which also provides power to the camera 10. . . . The camera 10 can acquire both still and motion images." (Endsley 471 at 2:49-59.)

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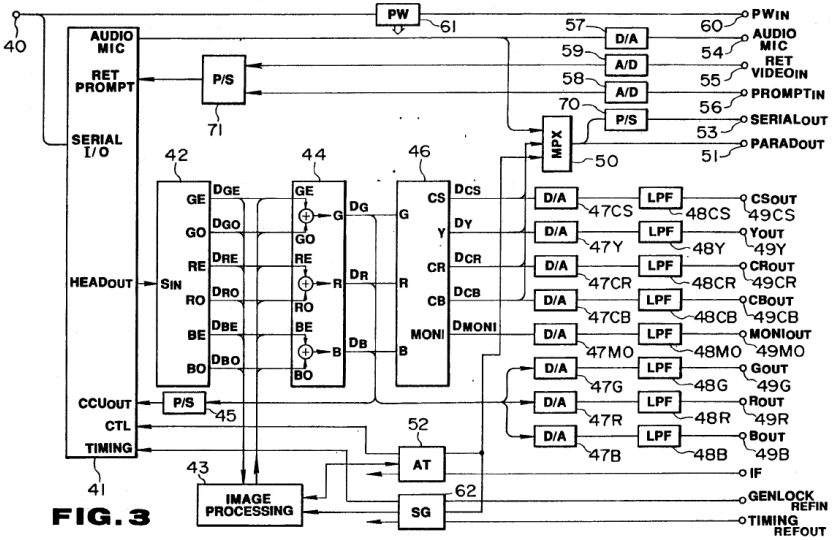
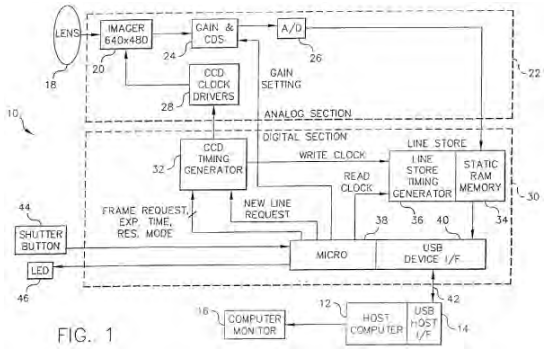
Claims	**Asaida 782**	**in combination with one or more of the following references**
	 FIG. 3 Asaida 782 (Figure 3)	 FIG. 1 Endsley 471 (Figure 1) To the extent the preamble is limiting, Dowdy 082 discloses "[a] video imaging system." "The invention relates to camera heads for use with remote video display systems such as video endoscopy systems, borescopes, and other devices." (Dowdy 082 at 1:10-12.) "Referring to FIG. 1, a video endoscopy or borescope system 10 includes a camera head 12 and a camera processor 14. Camera head 12 includes an endoscope 16 for insertion into a region such as a body cavity, and an imaging device, such as a CCD 18, that produces electrical signals representative of an optical image at the distal end of endoscope 16. Camera processor 14 processes the electrical signals produced by camera head 12 to generate a video image that is displayed on a video monitor 20." (Dowdy 082 at 3:24-

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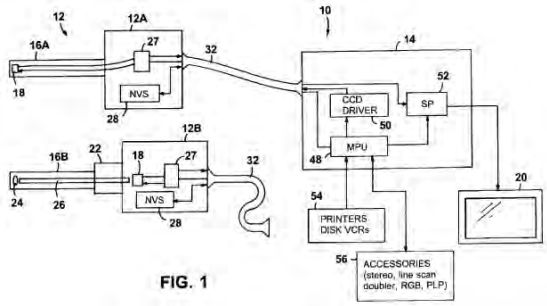
Claims	**Asaida 782**	**in combination with one or more of the following references**
		32.)  FIG. 1 Dowdy 082 (Figure 1) To the extent the preamble is limiting, Oshima 212 discloses "[a] video imaging system. "An endoscope system 1 in accordance with the first embodiment of the present invention shown in FIG. 1 consists broadly of an endoscope 2, and connected apparatuses (or peripheral equipment) to be selectively connected to the endoscope. The connected apparatuses include an image processing apparatus 3A, an image processing apparatus 3B, a cleaning apparatus 3C, a filing apparatus 3D, a monitor 4 a, an image recording apparatus 5 a, a filing apparatus 6 a, a monitor 4 b, an image recording apparatus 5 b, a filing apparatus 6 b, a filing apparatus 6 c, and a monitor 4 d. The image processing apparatus 3A has the ability to communicate with the endoscope 2. . . ." (Oshima 212 at 5:15-26.)

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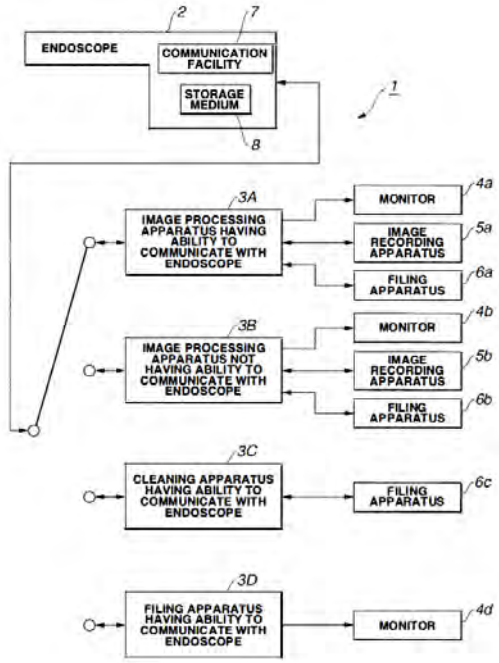
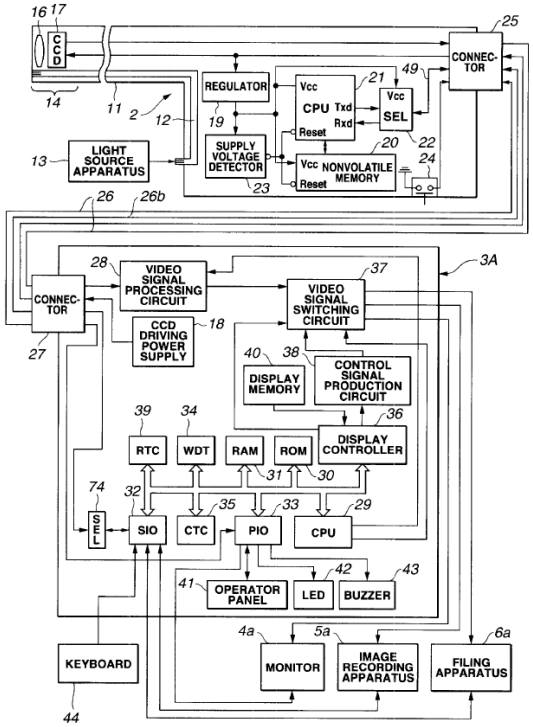
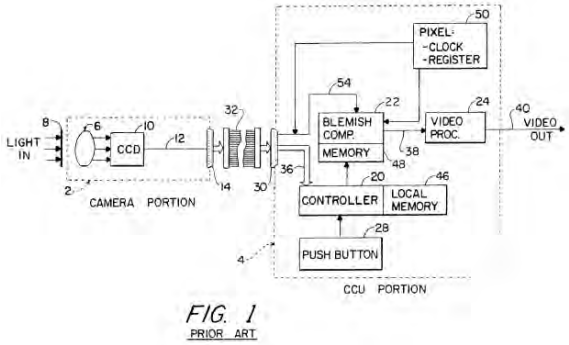
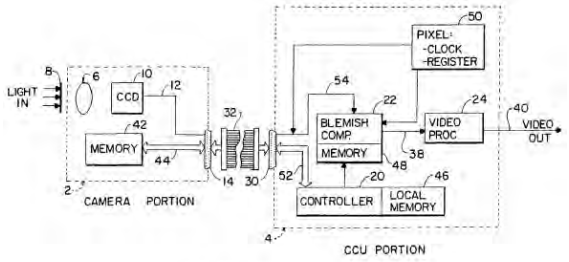
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Oshima 212 (Figure 1) "FIG. 2 is a block diagram showing in detail the endoscope 2 and the image processing apparatus 3A having the communicating ability which are employed in the present embodiment." (Oshima 212 at 6:34-37.)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Oshima 212 (Figure 2) To the extent the preamble is limiting, Zu 391 discloses "[a] video imaging system." "This invention relates to compensating for CCD blemishes in video cameras and ore particularly to cameras that are designed to be used interchangeably with camera control units, notably but not exclusively video cameras that are

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		incorporated in endoscopes for use with medical imaging systems." (Zu 391 at 1.) "Fig. 2 illustrates the invention. Except as described hereinafter, the system shown in Fig. 2 incorporates the same elements and the same functions as the system of Fig. 1, and identical elements are identified by the same numerals." (Zu 391 at 7.)  FIG. 1 PRIOR ART Zu 391 (Figure 1)  FIG. 2

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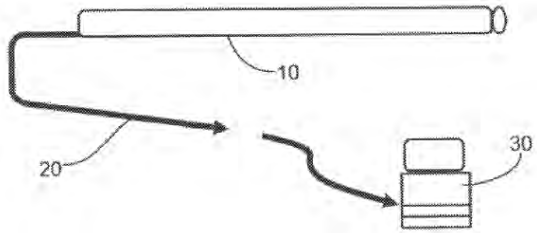
Claims	**Asaida 782**	**in combination with one or more of the following references**
		Zu 391 (Figure 2) To the extent the preamble is limiting, Adler 940 discloses "[a] video imaging system." "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope. The skilled person will appreciate that the wire connection 20 may be an optical connection or may instead use RF or a like means of wireless communication. The miniature endoscopic front-end 10 may be designed for connection to any standard PC input (the USB input for example)." (Adler 940 at 9:24-38.) 

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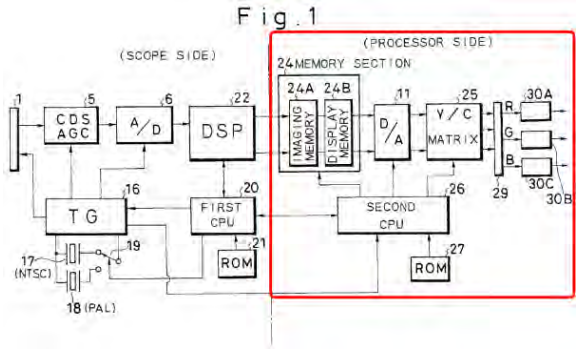
Claims	**Asaida 782**	**in combination with one or more of the following references**
		Adler 940 (Figure 1)
a camera control unit processing a continuous stream of digital video data;	"FIG. 3 is a block diagram showing an embodiment of a camera control unit of the video camera shown in FIG. 1." (Asaida 782 at 3:50-52.) "The video camera according to the present invention is constituted by the above mentioned camera head unit shown in FIG. 1 and the camera control unit CCU arranged and constituted as shown in FIG. 3." (Asaida 782 at 8:1-4.) "The camera control unit CCU, constituting part of the video camera according to the present invention, is provided with a serial input/output port 40, as shown in FIG. 3, which is connected to the serial input/output port 10 of the camera head unit by an optical fiber cable, not shown, constituting transmission means." (Asaida 782 at 8:5-10.)	"[O]n the external processor side, a memory section 24 equipped with an imaging memory 24A and a display memory 24B, a D/A converter 11, a brightness/color signal (Y/C) matrix circuit 25, a second CPU 26 for controlling these circuits, and a ROM 27 storing the setting data for the control meeting the selected television system of the NTSC or the PAL are provided." (Okada 852 at 4:34-40.) Fig. 1  Okada 852 (Figure 1) "The system includes a camera 10 connected to a host computer 12 via a USB (universal serial bus) cable 42 connected to a USB digital host interface 14, which also provides power to the camera 10. . . . The camera 10 can acquire both still and motion images. The camera data is processed by the host computer 12 to create final images that can be displayed on a computer monitor 16, e.g., transmitted

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Claims	**Asaida 782**	**in combination with one or more of the following references**

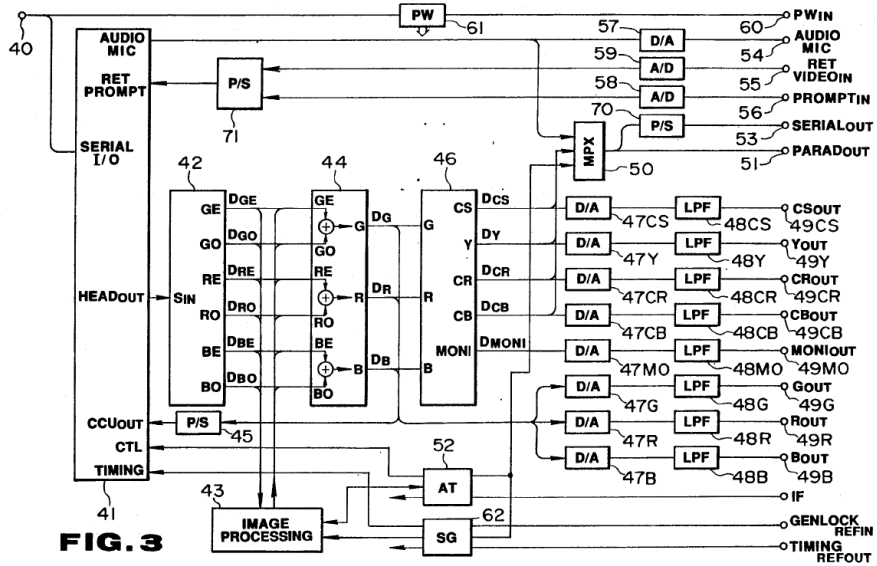

FIG. 3

Asaida 782 (Figure 3)

along with audio as part of a 'computer videoconference', etc." (Endsley 471 at 2:50-63.)

"The host computer 12 controls the camera operation. It can instruct the camera 10 when to take still or motion pictures, and set the electronic exposure time via the CCD timing generator 32, and set the analog gain in the CDS/gain block 24 from the microprocessor 38." (Endsley 471 at 3:54-58.)

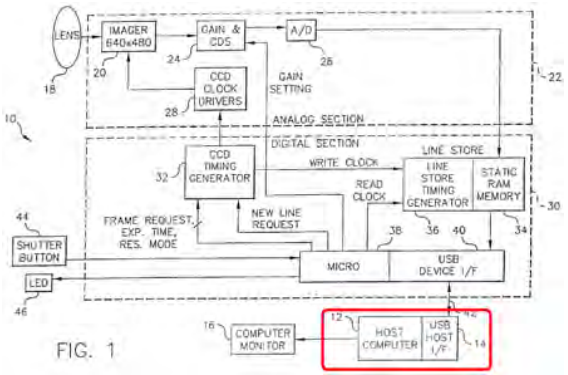

FIG. 1

Endsley 471 (Figure 1)

"Referring to FIG. 1, a video endoscopy or borescope system 10 includes a camera head 12 and a camera processor 14. Camera head 12 includes an endoscope 16 for insertion into a region such as a body cavity, and an imaging device, such as a CCD 18, that produces electrical signals representative of an optical image at the distal end of endoscope 16. Camera processor 14 processes the electrical signals produced by camera head 12 to generate a video image that

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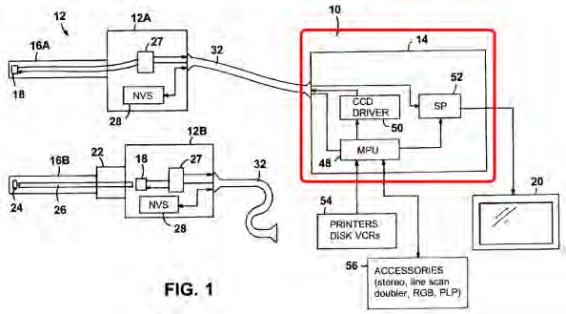
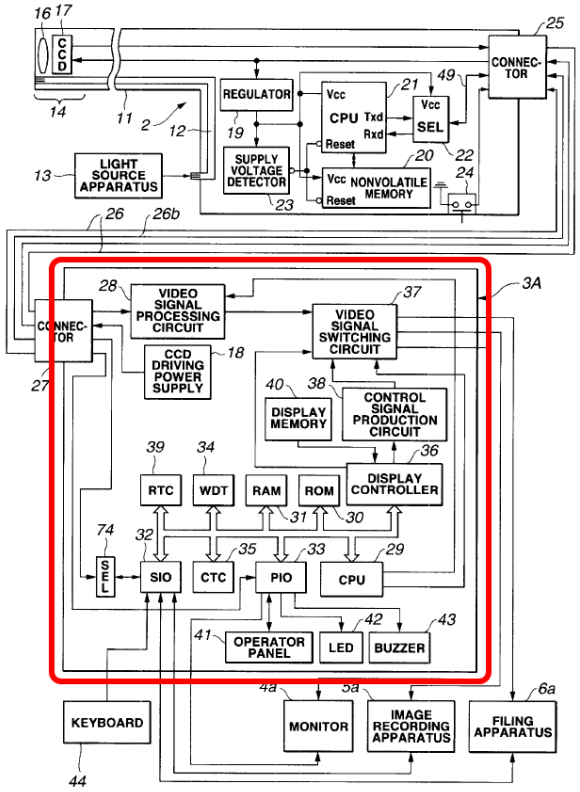
Claims	**Asaida 782**	**in combination with one or more of the following references**
		is displayed on a video monitor 20." (Dowdy 082 at 3:24-32.)  FIG. 1 Dowdy 082 (Figure 1) "FIG. 2 is a block diagram showing in detail the endoscope 2 and the image processing apparatus 3A having the communicating ability which are employed in the present embodiment." (Oshima 212 at 6:34-37.)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Oshima 212 (Figure 2) "The image processing apparatus 3A consists broadly of a CCD driving power supply 18, a video signal processing circuit 28, a CPU 29, a ROM 30, a RAM 31, a serial controller (S10) 32, a parallel communication controller (PIO) 33, a watchdog timer (WDT) 34, a counter timer

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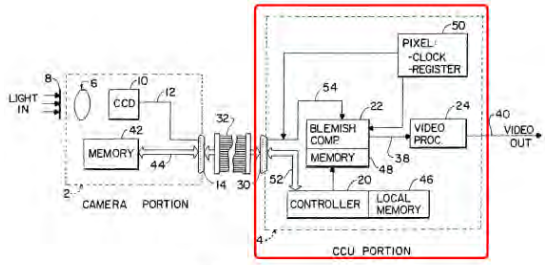
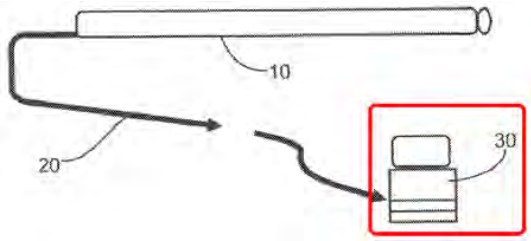
Claims	**Asaida 782**	**in combination with one or more of the following references**
		(CTC) 35, a display controller 36, a display memory 40, a video signal switching circuit 37, a control signal production circuit 38, a real-time clock (RTC) 39, an operator panel 41, an LED 42, a buzzer 43, and a light adjustment control unit. The CCD driving power supply 18 applies a voltage to the CCD 17 in the endoscope 2. The video signal processing circuit 28 processes a video signal resulting from photoelectric conversion performed by the CCD 17. The CPU 29 carries out a plurality of arithmetic operations." (Oshima 212 at 7:15-27.) "Figure 1 illustrates a prior art video system comprising a camera 2 and a CCU 4. . . . The CCU 4 comprises a controller 20 with local non-volatile digital memory 46, a blemish compensator 22 with associated volatile digital memory 48, a video signal processor 24, a pixel clock/pixel address register 50, a push-button interface and mode selector 28 for directing operation of controller 20." (Zu 391 at 3.)  FIG. 2

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		Zu 391 (Figure 2) "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope." (Adler 940 at 9:24-33.) "The software included with processing device 30 processes the output of the miniature endoscopic front-end 10. The software may typically control transfer of the images to the monitor of the PC 30 and their display thereon including steps of 3D modeling based on stereoscopic information as will be described below, and may control internal features of the endoscopic front end 10 including light intensity, and automatic gain control (AGC), again as will be described below." (Adler 940 at 9:39-47.) 

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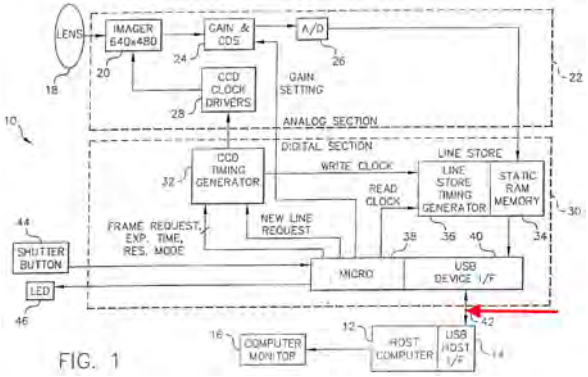
Claims	**Asaida 782**	**in combination with one or more of the following references**
		Adler 940 (Figure 1)
a cable, connected to said camera control unit, for transmitting the stream of digital video data to said camera control unit; and	"The camera control unit CCU, constituting part of the video camera according to the present invention, is provided with a serial input/output port 40, as shown in FIG. 3, which is connected to the serial input/output port 10 of the camera head unit by an optical fiber cable, not shown, constituting transmission means." (Asaida 782 at 8:5-10 (emphasis added).)	"The system includes a camera 10 connected to a host computer 12 via a USB (universal serial bus) cable 42 connected to a USB digital host interface 14, which also provides power to the camera 10. . . . The camera 10 can acquire both still and motion images. The camera data is processed by the host computer 12 to create final images that can be displayed on a computer monitor 16, e.g., transmitted along with audio as part of a 'computer videoconference', etc." (Endsley 471 at 2:50-63.) "The USB cable 42 includes four wires, one pair for sending data to and from the host computer 12, and a second pair to supply power to the camera 10 from the host." (Endsley 471 at 3:46-48.)  FIG. 1

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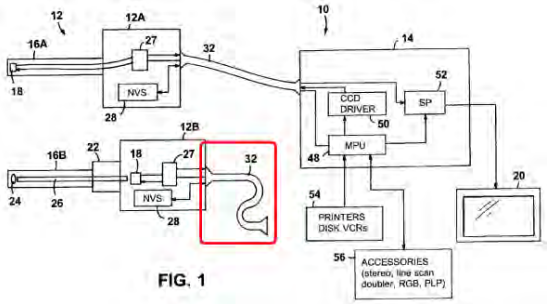
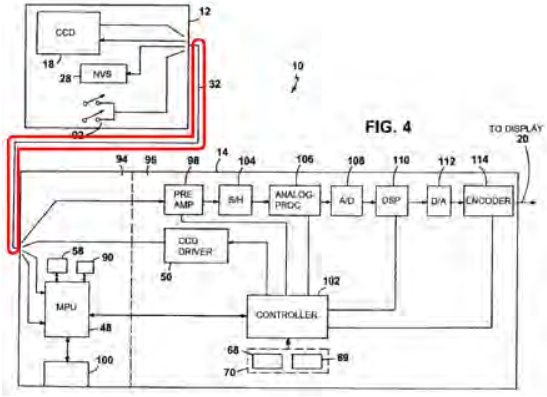
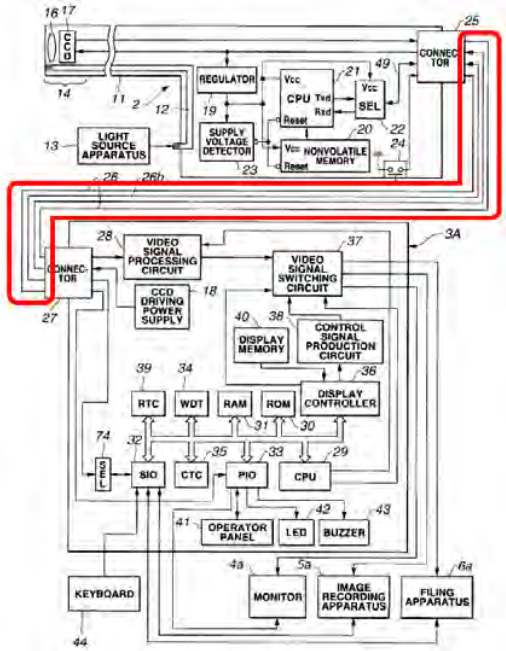
Claims	**Asaida 782**	**in combination with one or more of the following references**
		Endsley 471 (Figure 1) "Referring to FIG. 4, in a more detailed view, camera head 12 includes CCD 18 (located, as discussed, either in the head or at the tip of the endoscope), NVS 28 and a set of button switches 92 for system control, and camera processor 14 includes a camera controller 94 and a signal processor 96. Cable 32, which connects camera head 12 to camera processor 14, carries drive signals from CCD driver 50 in signal processor 96, electrical signals from CCD 18 to a preamplifier 98 in signal processor 96, data between NVS 28 and MPU 48 in camera controller 94, and signals from button switches 92 to MPU 48." (Dowdy 082 at 6:48-58.)  FIG. 1 Dowdy 082 (Figure 1)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Dowdy 082 (Figure 4) "The connector 25 of the endoscope 2 is linked to a connector 27 of the image processing apparatus 3A by a cable 26." (Oshima 212 at 7:11-13.)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Oshima 212 (Figure 2) "The CCU 4 also comprises an input connector 30 whereby the CCU may be coupled to camera output connector 14 via a suitable cable 32." (Zu 391 at 3.)

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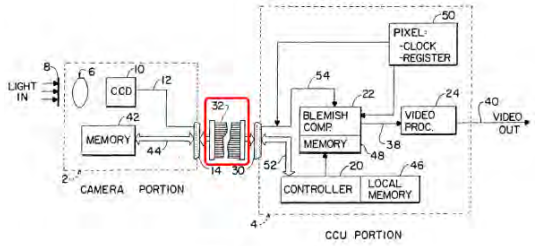
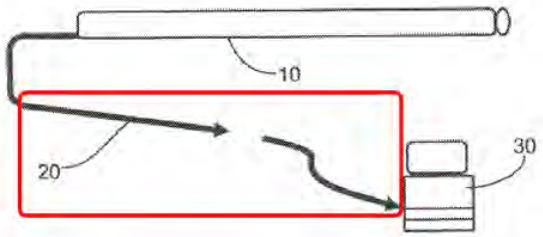
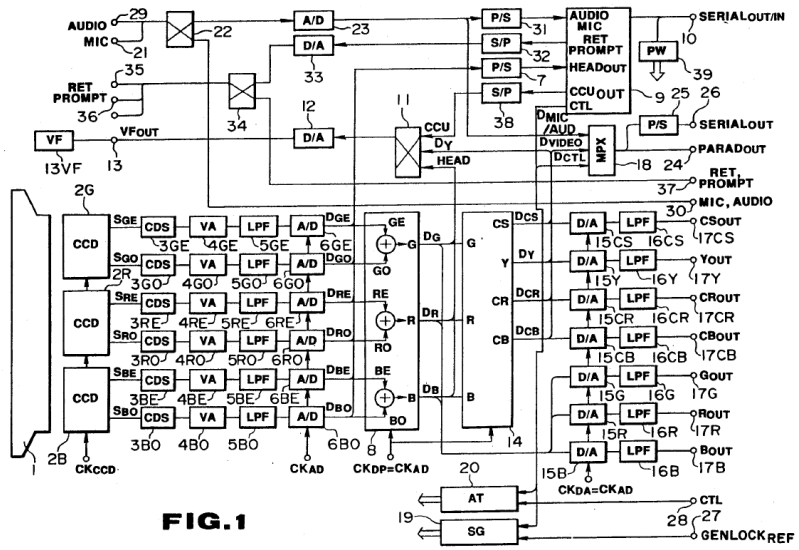
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 FIG. 2 Zu 391 (Figure 2) "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope. The skilled person will appreciate that the wire connection 20 may be an optical connection or may instead use RF or a like means of wireless communication. The miniature endoscopic front-end 10 may be designed for connection to any standard PC input (the USB input for example)." (Adler 940 at 9:24-38.)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Adler 940 (Figure 1)
a camera head, connected to said cable, for providing the stream of digital video data, said camera head including;	"FIG. 1 is a block diagram showing an embodiment of a camera head unit of a video camera according to the present invention." (Asaida 782 at 3:44-46.)  FIG.1	"In FIG. 1 and FIG. 2, the circuit configuration of an electronic endoscope according to the embodiment is shown. In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having a number of scanning lines or the like suitable for the scanning line of the NTSC system, and to this CCD 1, a timing generator 16 is connected, and to this timing generator 16, an NTSC crystal oscillator 17, a PAL crystal oscillator 18, and a switching device 19 are provided. Furthermore, a first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU 20, either of the oscillators 17, 18 is selected." (Okada 852 at 4:4-15.)

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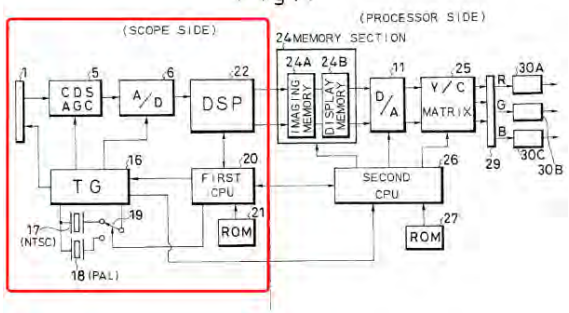
Claims	**Asaida 782**	**in combination with one or more of the following references**
	Asaida 782 (Figure 1) "The encoder/decoder 9 encodes the serial data, that is, the camera output data $HEAD_{OUT}$, supplied from the P/S converter 7, and outputs the encoded data at a serial input/output port 10 over an optical fiber cable, not shown." (Asaida 782 at 5:45-49.) "Thus, with the present video camera unit, the two-line-concurrent three-color imaging output signals S_{RO}, S_{RE}, S_{GO}, S_{GE}, S_{BO} and S_{BE}, obtained by the solid-state image sensors 2R, 2G, and 2B, are changed by the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE into two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}. The two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, are converted by the P/S converter 7 into serial data as the camera output data $HEAD_{OUT}$, which are serially outputted at the serial input/output port 10 by means of the encoder/decoder 9." (Asaida 782 at 5:50-61.)	Fig. 1  Okada 852 (Figure 1) "The system includes a camera 10 connected to a host computer 12 via a USB (universal serial bus) cable 42 connected to a USB digital host interface 14, which also provides power to the camera 10. . . . The camera 10 can acquire both still and motion images. The camera data is processed by the host computer 12 to create final images that can be displayed on a computer monitor 16, e.g., transmitted along with audio as part of a 'computer videoconference', etc." (Endsley 471 at 2:50-63.)

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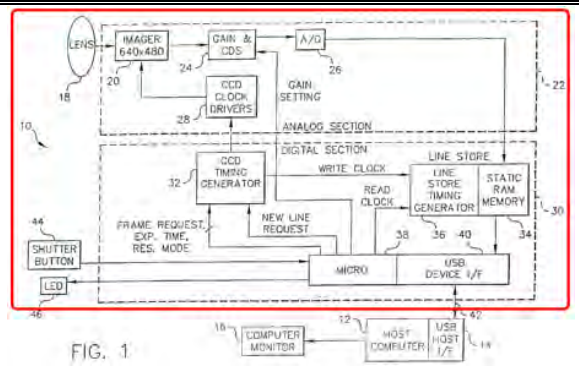
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 FIG. 1 Endsley 471 (Figure 1) "Referring to FIG. 1, a video endoscopy or borescope system 10 includes a camera head 12 and a camera processor 14. Camera head 12 includes an endoscope 16 for insertion into a region such as a body cavity, and an imaging device, such as a CCD 18, that produces electrical signals representative of an optical image at the distal end of endoscope 16. Camera processor 14 processes the electrical signals produced by camera head 12 to generate a video image that is displayed on a video monitor 20." (Dowdy 082 at 3:24-32.) "By varying parameters such as the type of endoscope, the endoscope mount, and the CCD optical format size, camera head 12 can be configured in numerous ways, all of which can produce different electrical signals to represent the same optical image. As illustrated in FIG. 1, camera head 12A includes an electronic endoscope 16A, while camera head

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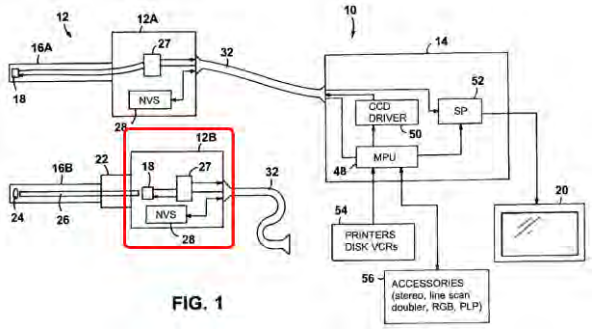
Claims	**Asaida 782**	**in combination with one or more of the following references**
		12B includes an optical endoscope 16B. Electronic endoscope 16A is integrally connected to camera head 12A and has a CCD 18 positioned behind focussing optics (not shown) at its distal end. By contrast, optical endoscope 16B has a mount 22 for attachment to camera head 12B, and includes an optical lens 24 positioned at its distal tip and an optical fiber 26 or relay lens assembly that transmits an image from optical lens 24 to a CCD 18 positioned, with support circuitry 27, within camera head 16B." (Dowdy 082 at 3:33-47 (emphasis added).)  FIG. 1 Dowdy 082 (Figure 1) "Referring to FIG. 4, in a more detailed view, camera head 12 includes CCD 18 (located, as discussed, either in the head or at the tip of the endoscope), NVS 28 and a set of button switches 92 for system control, and camera processor 14 includes a camera controller 94 and a signal processor 96. Cable 32, which connects camera head 12 to camera

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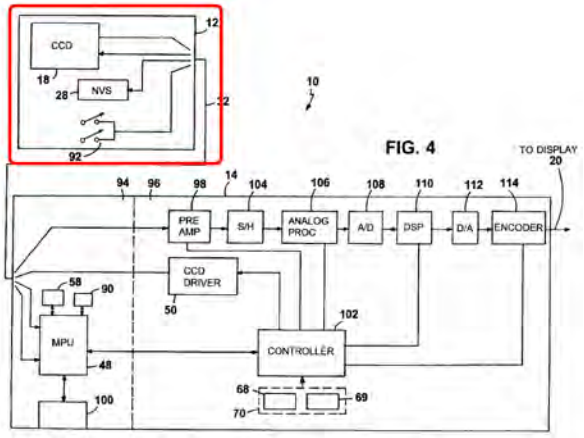
Claims	**Asaida 782**	**in combination with one or more of the following references**
		processor 14, carries drive signals from CCD driver 50 in signal processor 96, electrical signals from CCD 18 to a preamplifier 98 in signal processor 96, data between NVS 28 and MPU 48 in camera controller 94, and signals from button switches 92 to MPU 48." (Dowdy 082 at 6:48-58 (emphasis added).)  Dowdy 082 (Figure 4) "An endoscope system 1 in accordance with the first embodiment of the present invention shown in FIG. 1 consists broadly of an endoscope 2, and connected apparatuses (or peripheral equipment) to be selectively connected to the endoscope. The connected apparatuses include an image processing apparatus 3A, an image processing apparatus 3B, a cleaning apparatus 3C, a filing apparatus 3D, a monitor 4 a, an image recording apparatus 5

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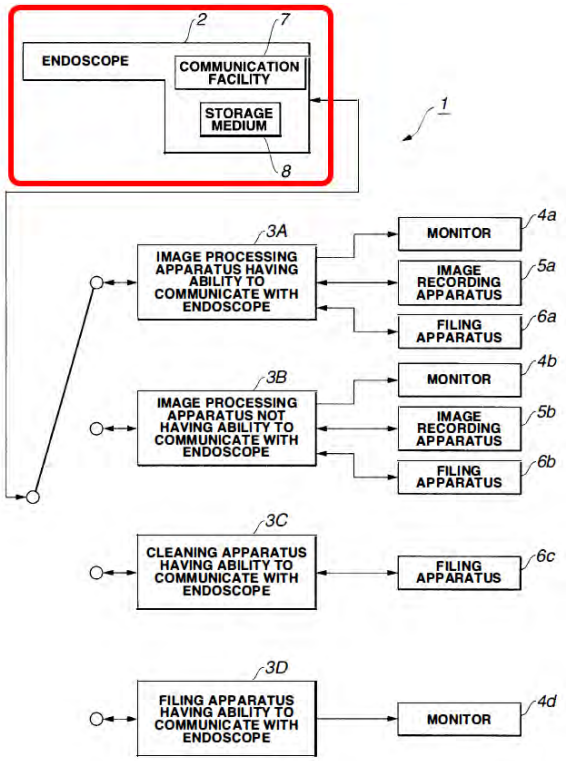
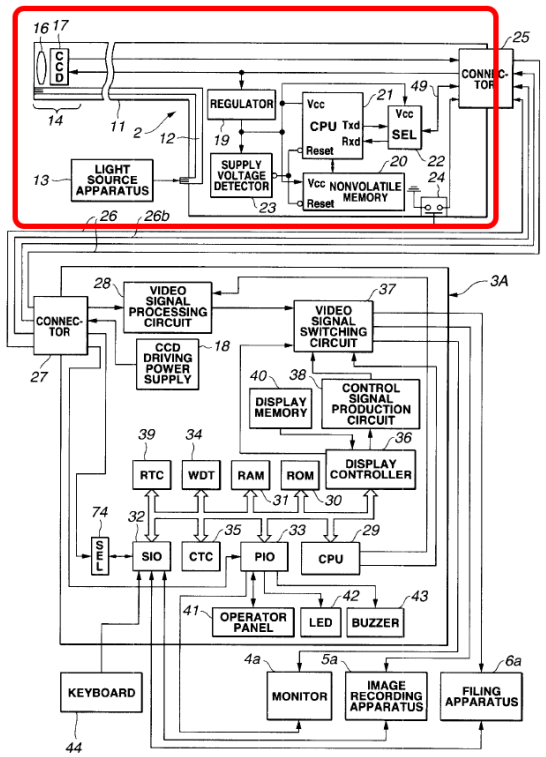
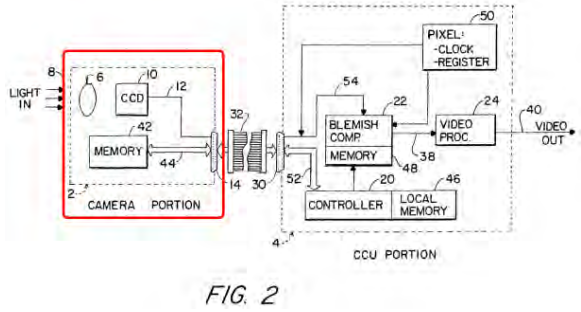
Claims	**Asaida 782**	**in combination with one or more of the following references**
		a, a filing apparatus 6 a, a monitor 4 b, an image recording apparatus 5 b, a filing apparatus 6 b, a filing apparatus 6 c, and a monitor 4 d. The image processing apparatus 3A has the ability to communicate with the endoscope 2. . . ." (Oshima 212 at 5:15-26.)  Oshima 212 (Figure 1)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		"FIG. 2 is a block diagram showing in detail the endoscope 2 and the image processing apparatus 3A having the communicating ability which are employed in the present embodiment." (Oshima 212 at 6:34-37.)  Oshima 212 (Figure 2) "The connector 25 of the endoscope 2 is linked to a

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		connector 27 of the image processing apparatus 3A by a cable 26." (Oshima 212 at 7:11-13.) "Figure 1 illustrates a prior art video system comprising a camera 2 and a CCU 4. The camera comprises an optical system 6 and a CCD array 10. The latter produces a video signal output when it is illuminated with light via optical system 6. This video signal output is fed by an internal transmission bus 12 to an output connector 14 which forms part of the camera." (Zu 391 at 3.)  FIG. 2 Zu 391 (Figure 2) "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20

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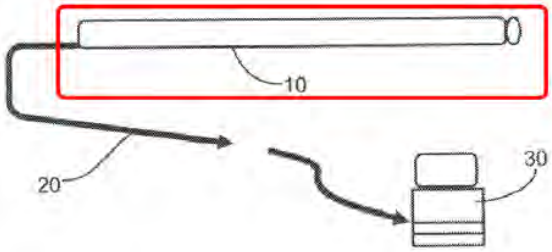
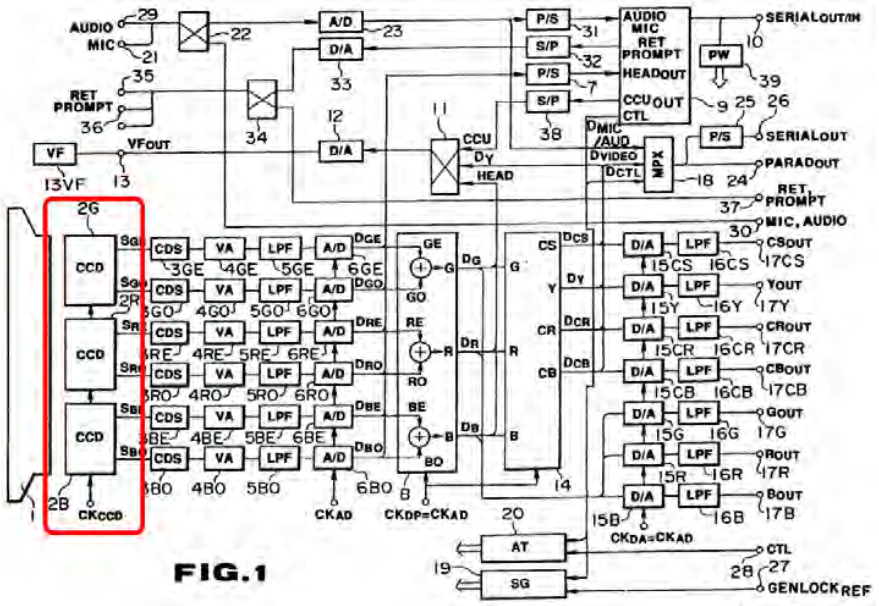
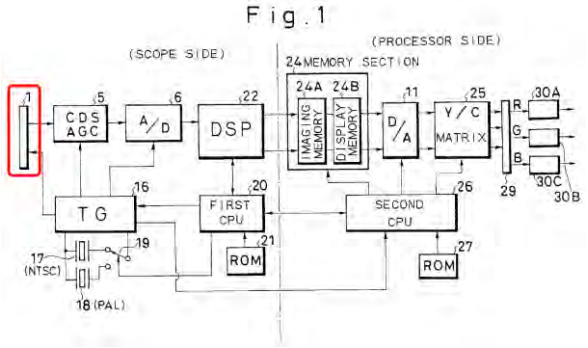
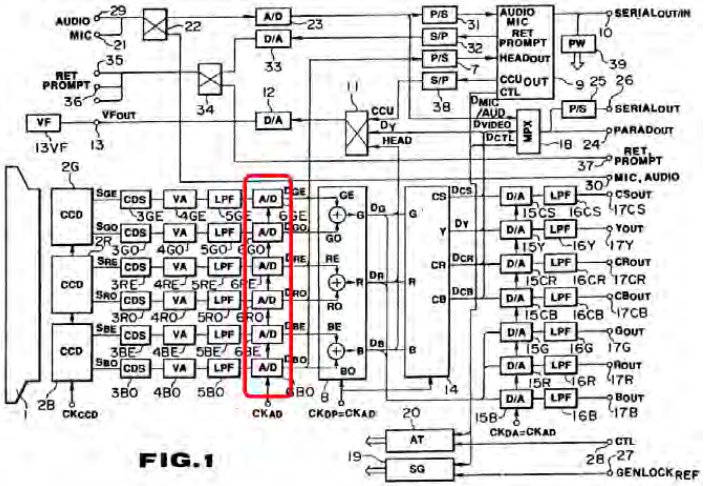
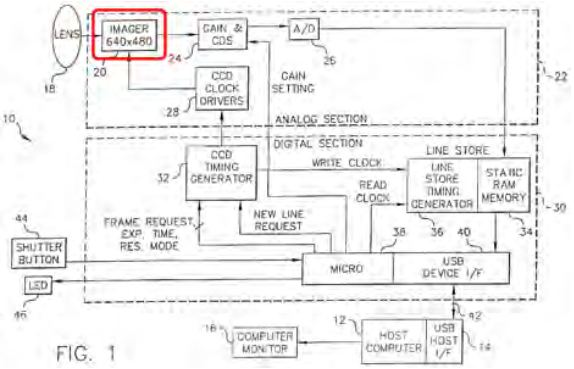
Claims	**Asaida 782**	**in combination with one or more of the following references**
		to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope. The skilled person will appreciate that the wire connection 20 may be an optical connection or may instead use RF or a like means of wireless communication. The miniature endoscopic front-end 10 may be designed for connection to any standard PC input (the USB input for example)." (Adler 940 at 9:24-38.)  Adler 940 (Figure 1)
an imager, for generating the stream of digital video data;	"In the camera head unit, shown in FIG. 1, the present invention includes a three CCD solid state color imaging device in which the imaging light from an object in a field of view is separated by an imaging pickup device 1 into three primary color components and in which three primary color object images are produced by three solid state imaging sensors 2R, 2G and 2B." (Asaida 782 at 4:9-15.)	"In FIG. 1 and FIG. 2, the circuit configuration of an electronic endoscope according to the embodiment is shown. In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having a number of scanning lines or the like suitable for the scanning line of the NTSC system, and to this CCD 1, a timing generator 16 is connected, and to this timing generator 16, an NTSC crystal oscillator 17, a PAL crystal oscillator 18, and a switching device 19 are provided. Furthermore, a first CPU 20 is provided, which controls the total while controlling this

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
	 FIG.1 Asaida 782 (Figure 1) "The two-line-concurrent three-color imaging output signals S_{RO}, S_{RE}, S_{GO}, S_{GE}, S_{BO} and S_{BE}, processed for level adjustment by the level adjustment circuits 4RO, 4RE, 4GO, 4GE, 4BO and 4BE, are transmitted by means of low-pass filters 5RO, 5RE, 5GO, 5GE, 5BO and 5BE, respectively, to A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, functioning as analog/ digital converting means, respectively." (Asaida 782 at 5:14-22.) "A driving clock CK_{AD} having a frequency four times the frequency of the color subcarrier frequency f_{SC}, or $4f_{SC}$, is supplied to the A/D	switching device 19, and by the control of this first CPU 20, either of the oscillators 17, 18 is selected." (Okada 852 at 4:4-15.)  Okada 852 (Figure 1) "The camera 10 includes an optical section 18 from imaging light from a subject upon an electronic image sensor 20. A preferred image sensor is a Kodak KAI-0320CM interline transfer, progressive-scan charge-coupled-device (CCD) image sensor with a usable active image area having 640 columns and 480 rows of color photoelements arranged in the well-known Bayer color filter array patters shown in FIG. 2 (see U.S. Pat. No. 3,971,065 for further description of the Bayer pattern). As shown in FIG. 2, the sensor 20 includes light shielded vertical registers 50 and a horizontal readout register 52. Details of a single photoelement 54 are shown in FIG. 3. Each photoelement 54 includes a light-sensitive photodiode 56 supported on a substrate 58 adjacent the light-

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
	converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, by means of a timing generator, not shown. The A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE digitize the two-line-concurrent three-color imaging output signals S_{RO}, S_{RE}, S_{GO}, S_{GE}, S_{BO} and S_{BE} with the $4f_{sc}$ driving clock CK_{AD} to produce two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, respectively. The two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, produced by the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, are supplied to a parallel/serial converter (P/S converter) 7 and to a signal processing section 8." (Asaida 782 at 5:23-37.)  FIG.1 Asaida 782 (Figure 1)	shielded vertical register 50." (Endsley 471 at 2:66-3:12.)  FIG. 1 Endsley 471 (Figure 1) "An analog section 22 in the camera 10 includes the sensor 20, a CDS/gain block 24 for performing correlated double sampling (CDS) and setting the analog gain, an analog-to-digital (A/D) converter 26 for converting the analog output signal from the CCD sensor 20 to, e.g., an 8-bit digital signal, and CCD clock drivers 28 for clocking the sensor 20." (Endsley 471 at 3:13-18.)

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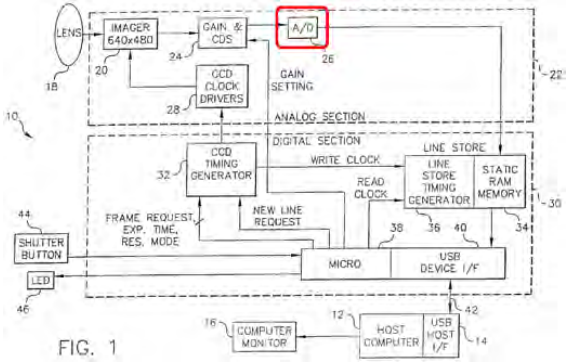
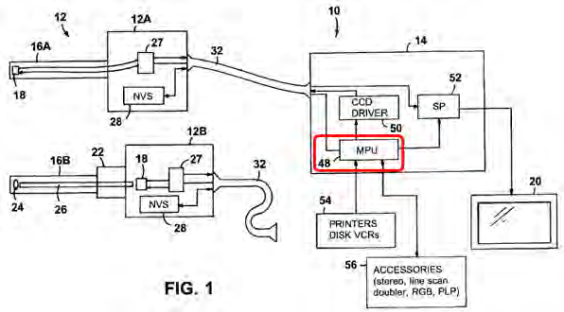
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Endsley 471 (Figure 1) "As shown in FIG. 1, camera processor 14 includes a microprocessing unit ("MPU") 48, a CCD driver 50, and signal processing ("SP") circuitry 52. In operation, MPU 48 provides control to CCD driver 50 for transmitting driving signals to CCD 18 in camera head 12. In response to the driving signals, CCD 18 produces electrical signals representing an image of objects within the field of view of CCD 18, and transmits the electrical signals to signal processing circuitry 52. Signal processing circuitry 52 processes the electrical signals from CCD 18 and converts them to video signals for displaying the image on video monitor 20." (Dowdy 082 at 4:60-5:3.)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 FIG. 1 Dowdy 082 (Figure 1) "Referring also to FIG. 3, MPU 48 uses the information stored in NVS 28 to control the operation of CCD driver 50 and signal processing circuitry 52. When the user connects cable 32 of camera head 12 to camera processor 14, and, if necessary, powers up video endoscopy system 10, MPU 48 detects the connection and responds by downloading the information from NVS 28 into a memory 58, such as a RAM, of MPU 48 (step 200). MPU 48 reads the stored information out of NVS 28 through a serial data link in cable 32 that includes a CLOCK line 60 controlled by MPU 48 and a DATA line 62 that is shared by NVS 28 and MPU 48." (Dowdy 082 at 5:9-19.) "MPU 48 communicates with signal processing circuitry 52 through a bidirectional serial data link that includes a CLOCK line 80 controlled by MPU 48 and a DATA line 82 that is shared by MPU 48 and signal processing circuitry 52. MPU 48 also controls an ENABLE line 84 that activates

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		external control of signal processing circuitry 52." (Dowdy 082 at 6:1-6.) "After modifying the values of table entries 72-78 received from signal processing circuitry 52, MPU 48 transmits the updated values to signal processing circuitry 52 (step 218). When entries from NVS 28 reflect replacement values for entries in lookup table 68, MPU 48 transmits the replacement values (step 218) without requesting values from signal processing circuitry and modifying those values (steps 208-216)." (Dowdy 082 at 6:18-25.) "After signal processing circuitry 52 receives the updated values from MPU 48 (step 220), signal processing circuitry 52 uses the updated values in processing the electrical signals from CCD 18 for display on video monitor 20 (step 222). That is, signal processing circuitry 52 uses the updated values in locations 69—rather than the nominal values from lookup table 68—in performing the conversion of the electrical signals from CCD 18 to video signals." (Dowdy 082 at 6:26-33.) "Referring to FIG. 4, in a more detailed view, camera head 12 includes CCD 18 (located, as discussed, either in the head or at the tip of the endoscope), NVS 28 and a set of button switches 92 for system control, and camera processor 14 includes a camera controller 94 and a signal processor 96. Cable 32, which connects camera head 12 to camera processor 14, carries drive signals from CCD driver 50 in signal processor 96, electrical signals from CCD 18 to a

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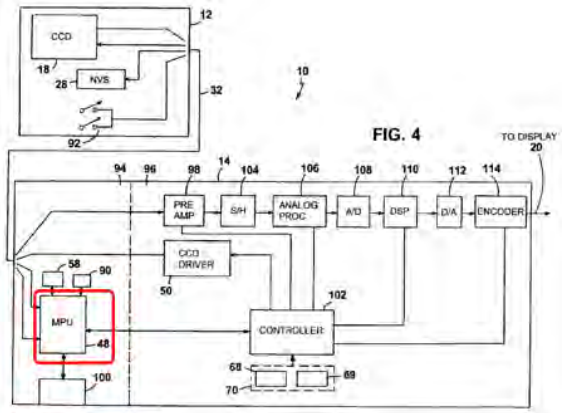
Claims	**Asaida 782**	**in combination with one or more of the following references**
		preamplifier 98 in signal processor 96, data between NVS 28 and MPU 48 in camera controller 94, and signals from button switches 92 to MPU 48." (Dowdy 082 at 6:48-58.)  Dowdy 082 (Figure 4) "MPU 48 controls signal processor 96 in response to signals from button switches 92 and signals from controls in a front panel 100 of camera controller 94. The controls in front panel 100 allow the user of video endoscopy system 10 to configure button switches 92 to perform desired functions. Thus, for example, button switches 92 could be configured to cause signal processor 96 to pause the video image displayed at video monitor 20 (FIG. 1). MPU 48 also displays system parameters at front panel 100, interacts with NVS 28 by downloading information about camera head 12 and updating run time information in NVS 28, updates signal processing

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		parameters in light of the information about camera head 12, and communicates with signal processor 96, all as discussed above." (Dowdy at 6:59-7:5.) Although MPU 48 is located in camera processor 14, it is contained within camera controller 94 which is independent of camera processor 96. Because camera controller 94 and camera processor 96 are independent units housed within camera processor 14, camera controller 94 (and as a result, MPU 48) could have been located in camera head 12. Locating camera controller 94 in the camera head 12 would have been a design option attractive to one of ordinary skill in the art looking to minimize communication circuitry between NVS 28 and MPU 48, as both would be housed within camera 12. "The illuminated object is imaged by a solid-state imaging device located on an image plane, for example, a charge-coupled device (CCD) 17 through an objective 16 locked in an observation window formed in the distal part 14. The CCD 17 photoelectrically converts the optical image." (Oshima 212 at 6:49-53.)

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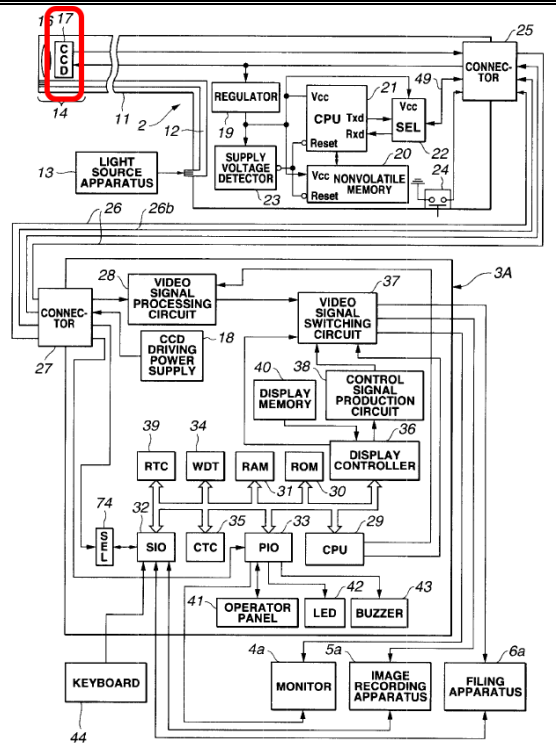
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Oshima 212 (Figure 2) "Reference is now made to FIG. 2, which is an internal block diagram of an endoscope according to a preferred embodiment of the present invention. A miniature endoscope 40 is connected by a wire 42 to an adapter 44. The endoscope 40 comprises an image sensor 46 which may typically comprise a CMOS or CCD or like sensing technology, an

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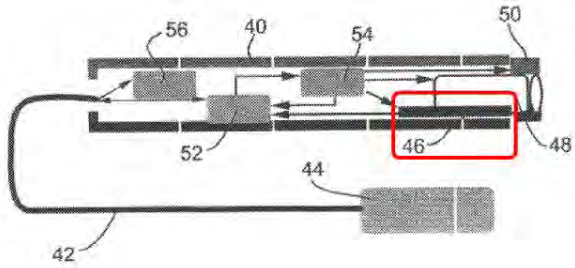
Claims	**Asaida 782**	**in combination with one or more of the following references**
		optical assembly 48, a light or illumination source 50, communication interface 52 and controller 54. The wired unit of FIG. 2 preferably includes a voltage regulator 56." (Adler 940 at 9:48-57.)  Adler 940 (Figure 2) "Reference is now made to FIG. 4, which is an schematic block diagram of the miniature endoscope according to a preferred embodiment of the present invention. Parts that are identical to those shown above are given the same reference numerals and are not referred to again except as necessary for an understanding of the present embodiment. Optical assembly 48 receives light, indicated by arrows 60, from an object being viewed. The light is processed by optical assembly 48, as will be explained below, to reach image sensor 46 were it is converted from photons into electrical signals. The electrical signals are digitized and passed to a transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Adler 940 at 10:7-

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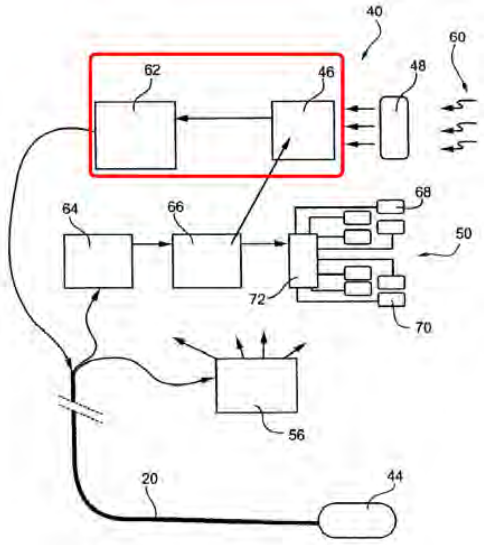
Claims	**Asaida 782**	**in combination with one or more of the following references**
		19 (emphasis added).)  Adler 940 (Figure 4) Because "the electrical signals are digitized and passed to a transmitting device 62" in the camera head, the camera head must contain a converter for converting an analog stream of video data into a stream of digital video data. "The present invention relates generally to the field of interface circuits, and more particularly, to interface circuitry for providing selectable single-ended and differential signal output from a CMOS image sensor to an external digital signal processor." (Chung 290 at 1:11-15.)

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		"One of the advantages of CMOS image sensors (CMOS imagers) over CCD imagers is that the CMOS imager chip can include digital signal processing circuitry. In practice, the signal processing is more often performed on a companion chip, in order to provide greater application flexibility. However, CMOS imagers often have integrated analog to digital converters to convert the analog signal to a digital bit stream that can be processed by the companion chip. The digitized information then must be transferred to companion chip or other external devices for picture storage, processing, or transmission." (Chung 290 at 1:17-27.) "FIG. 4 illustrates CMOS video imaging sensing circuitry according to the preferred embodiment disclosed in co-pending U.S. application Ser. No 09/062,343. This circuitry includes a CMOS image sensor chip 50 and an image processor chip 52. The CMOS image sensor chip 50 typically includes a number of light responsive CMOS pixel sensors which develop analog signals representative of an image. These analog signals are then A to D converted by the ADC circuit to form digital signals Din0, Din1 . . . Dinn. The image processor chip 52 includes a data processor 53 which performs various manipulations of the image data such as compression and color processing. The processor 53 may be software driven or a hardware embodiment." (Chung 290 at 2:14-26.)

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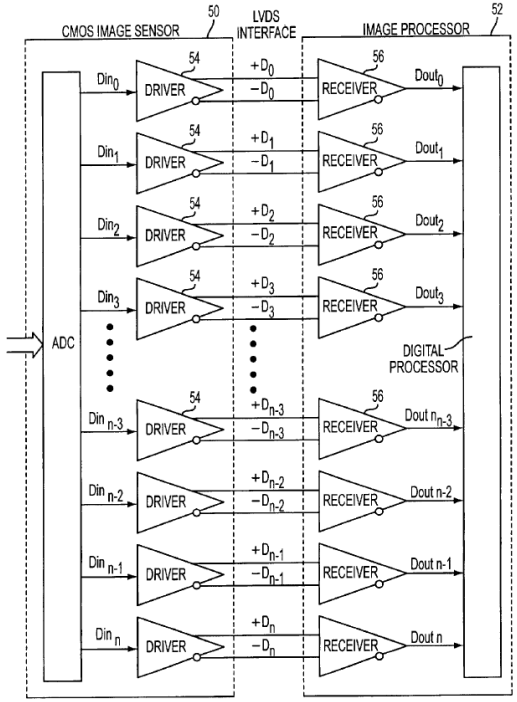
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Chung 290 (Figure 4)
a timing generator, generating a timing signal particular to said camera	"The three solid-state image sensors 2R, 2G and 2B, each formed as an above described two-line-concurrent reading high resolution CCD image sensor 2, are driven by a CCD driving circuit, not shown, using a driving clock CK_{CCD} having a frequency of, for example, 21.5 MHz." (Asaida 782 at 4:41-46.)	In FIG. 1 and FIG. 2, the circuit configuration of an electronic endoscope according to the embodiment is shown. In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having a number of scanning lines or the like suitable for the scanning line of the NTSC system, and to this CCD 1, a timing generator 16 is connected, and to this timing generator 16, an NTSC crystal

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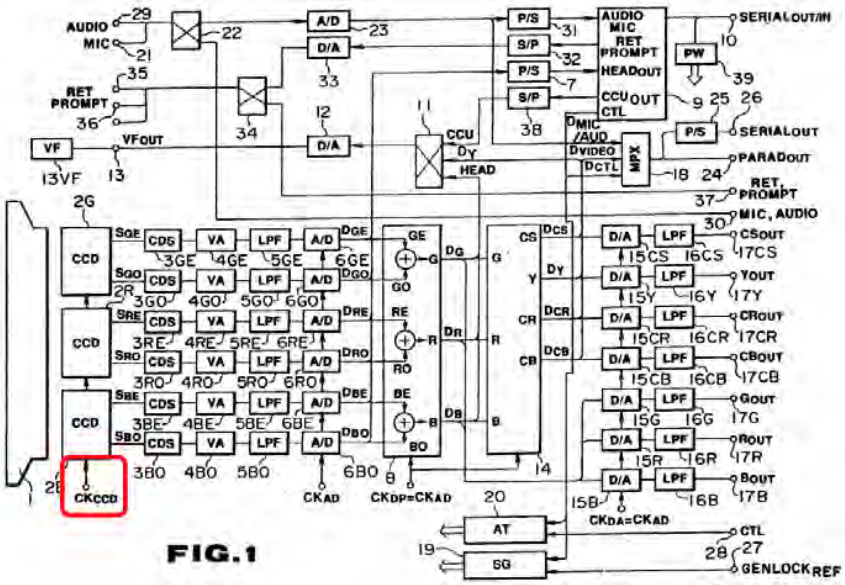
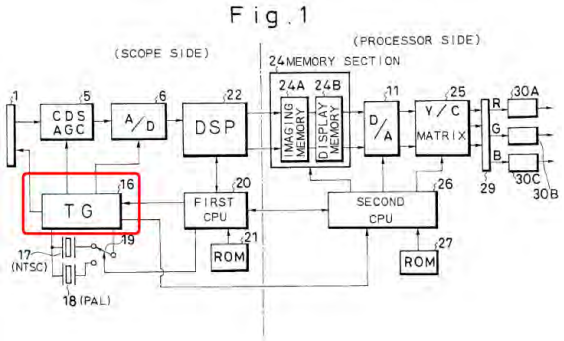
Claims	**Asaida 782**	**in combination with one or more of the following references**
head, the timing signal actuating said imager and sent to said camera control unit;	 FIG.1 Asaida 782 (Figure 1) "[W]ith the present video camera unit, the two-line-concurrent three-color imaging output signals S_{RO}, S_{RE}, S_{GO}, S_{GE}, S_{BO} and S_{BE}, obtained by the solid-state image sensors 2R, 2G, and 2B, are changed by the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE into two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}. The two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, are converted by the P/S converter 7 into serial data as the camera output data $HEAD_{OUT}$, which are serially outputted at the serial input/output port 10 by means of the encoder/decoder 9." (Asaida 782 at 5:50-61.)	oscillator 17, a PAL crystal oscillator 18, and a switching device 19 are provided. Furthermore, a first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU 20, either of the oscillators 17, 18 is selected." (Okada 852 at 4:4-15.)  Okada 852 (Figure 1) "A first example is configured like the above, and in the example, each television system can be selected by selective switches arranged at the processor or the like, and the state of selection of the switches can be grasped by the second CPU 26. Then, this second CPU 26 reads out the setting data of the selected system from the ROM 27 to set the processing contents of each circuit by this setting data. At the same time, the information of the selected system is also transmitted to the first CPU 20 on the scope side from this second CPU 26, and on this scope side, the selected setting data is read out

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Claims	**Asaida 782**	**in combination with one or more of the following references**
	"[T]he synchronizing circuit block 19 is supplied with a reference synchronizing signal $GENLOCK_{REF}$ for generator locking through synchronizing input terminal 27, while the control circuit block 20 is supplied with a control signal CTL through a control input terminal 28." (Asaida 782 at 7:16-21.) "The encoder/decoder 9 encodes the serial data supplied from P/S converters 7 and 31 and serially transmits the encoded serial data via the serial input/output port 10 to a camera control unit CCU described below, while also decoding various serial data transmitted from the camera control unit CCU to the serial input/output port 10, such as return video signals D_{RET}, prompter signals D_{PROMPT}, output signals CCU_{OUT} from the camera control unit CCU or control data D_{CTL}." (Asaida 782 at 7:35-43.) Thus, encoder/decoder 9 transmits either a separate timing signal or a timing signal embedded in the serial data signal received from P/S converter 7 (which originated from image sensors 2R, 2G, and 2B) and sent to the CCU through input/output port 10.	from the ROM 21 by the first CPU 20 to set the processing contents of each circuit, and further, either of the above oscillators 17, 18 is selected and set." (Okada 852 at 4:58-5:3.) "That is, if the NTSC system is selected, the NTSC system oscillator 17 is connected to the timing generator 16 by the switching circuit 19. In this timing generator 16, the oscillating signal with, for example, a frequency of 14.32 MHz generated in the oscillator 17 is divided to form the horizontal synchronization signal with a frequency of 15.734 kHz (fh1) and the vertical synchronization signal with a frequency of 59.94 Hz, and the driving pulse based on this is given to the CCD 1. Then, the picture signal extracted from this CCD 1 is subjected to the digital conversion after passing through the AGC circuit 5 for performing the correlative double sampling and the amplification processing, and as shown in FIG. 2, this digital picture signal is subjected to a specified processing by the DSP circuit 22, and it is supplied to the memory section 24 on the processor side." (Okada 852 at 5:4-20.)

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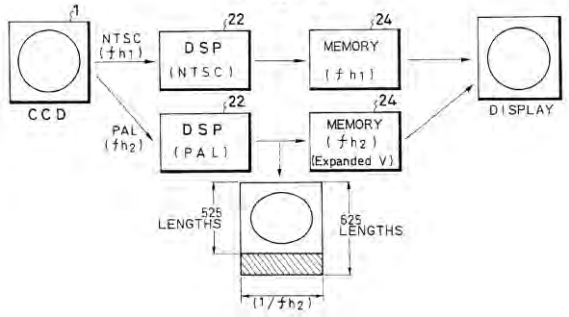
Claims	**Asaida 782**	**in combination with one or more of the following references**
		Fig. 2  Okada 852 (Figure 2) "In this memory section 24, the picture data is written in the imaging memory 24A in the timing of the synchronization signal formed in the timing generator 16, and after that, this picture data is read out in the same timing to be stored in the display memory 24B (as the data corresponding to the number of scanning lines of 525). The data of this display memory 24 is converted into the signals of R, G, and B from the brightness signal and the color difference signal in the Y/C matrix circuit 25 after being converted to the analog signal in the D/A converter 11. Then, each of these signals of R, G, and B is outputted to a monitor of the NTSC system through the isolation device 29 and the buffers 30 (A to C), and consequently, a picture of the NTSC system is displayed on the monitor." (Okada 852 at 5:21-35 (emphasis added).) Thus, the timing signal actuates the imager and is sent to the CCU.

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		"The sensor 20 is controlled by the timing generator 32 via the CCD clock driver 28. The timing generator 32 has a control input for receiving a new line request signal from the microprocessor 38; the new line request signal thus initiates the generation of clock signals to output a new line from the sensor 20. The digital data from the sensor 20 is temporarily stored in the static RAM line store memory 34, preferably a 64K bit static RAM memory (for example part number IDT7164 made by Integrated Device Technology, Inc.) which is controlled by a line store timing generator 36 so as to serve as a line store. Besides controlling the sensor 20, the CCD timing generator 32 also controls the line store write clock applied to the line store timing generator 36." (Endsley 471 at 3:24-36.) "The output of the line store memory 34 is connected to the host computer 12 via the USB device interface 40, which operates at a maximum data rate of 12M bits/sec." (Endsley 471 at 3:37-39.)

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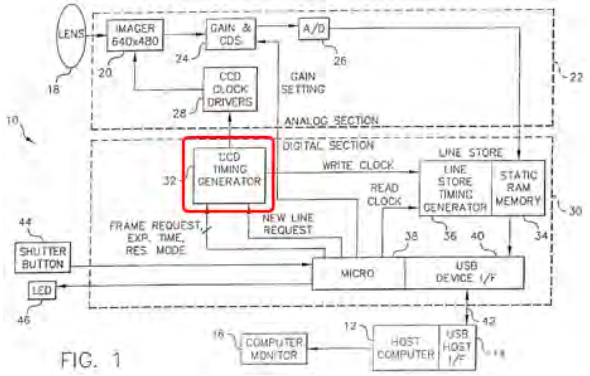
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Endsley 471 (Figure 1) The USB Device 40 transmits either a separate timing signal (*see, e.g.*, Section 5.10.2 of USB Spec. Rev. 1.0) or a timing signal embedded in the serial data signal sent to the CCU.
at least one digital serial driver;	"The encoder/decoder 9 encodes the serial data, that is, the camera output data $HEAD_{OUT}$, supplied from the P/S converter 7, and outputs the encoded data at a serial input/output port 10 over an optical fiber cable, not shown." (Asaida 782 at 5:45-49.) To the extent this element is not expressly disclosed, it is inherent in Asaida 782. It would be within the knowledge of one of ordinary skill in the art at the time of the alleged invention that transmitting a serial digital signal over a cable would necessarily require a driver to drive the signal and a receiver to receive the signal. Even if a piece of prior art does not expressly disclose a particular	To the extent this element is not expressly disclosed, it is inherent in Endsley 471 by virtue of disclosing and claiming USB as a communications medium. Specifically, section 7.1.1 of the USB Specification Revision 1.0 is directed to "USB Driver Characteristics": "The USB uses a differential output driver to drive the USB data signal onto the USB cable. The static output swing of the driver in its low state must be below the VOL of 0.3 V with a 1.5 kW load to 3.6 V and in its high state must be above the VOH of 2.8 V with a 15 kW load to ground as

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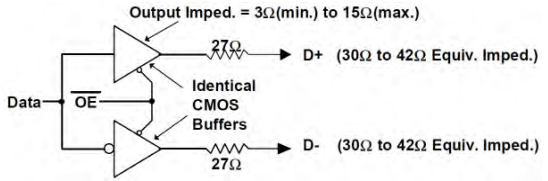
Claims	**Asaida 782**	**in combination with one or more of the following references**
	limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005) (citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)). Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	listed in Table 7-4. The output swings between the differential high and low state must be well balanced to minimize signal skew. Slew rate control on the driver is required to minimize the radiated noise and cross talk. The driver's outputs must support three-state operation to achieve bi-directional half duplex operation. High impedance is also required to isolate the port from downstream devices that are being hot inserted or which are connected but powered down. The driver must tolerate a voltage on the signal pins of -0.5 V to 3.8 V with respect to local ground reference without damage. It must tolerate this voltage for 10.0 µs while the driver is active and driving, and tolerate the condition indefinitely when the driver is in its high impedance state." (USB Spec. Rev. 1.0 at 111-13.)  USB Spec. Rev. 1.0 (Figure 7-1)

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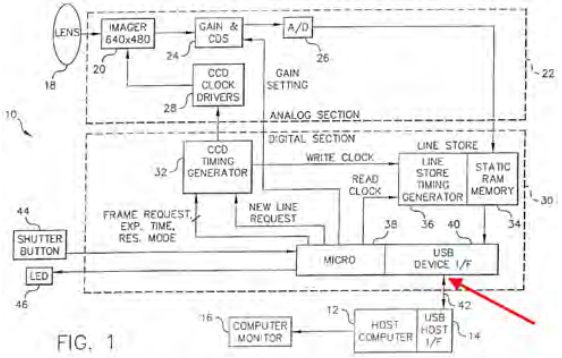
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Endsley 471 (Figure 1) "Reference is now made to FIG. 4, which is an schematic block diagram of the miniature endoscope according to a preferred embodiment of the present invention. Parts that are identical to those shown above are given the same reference numerals and are not referred to again except as necessary for an understanding of the present embodiment. Optical assembly 48 receives light, indicated by arrows 60, from an object being viewed. The light is processed by optical assembly 48, as will be explained below, to reach image sensor 46 were it is converted from photons into electrical signals. The electrical signals are digitized and passed to a transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Adler 940 at 10:7-19 (emphasis added).)

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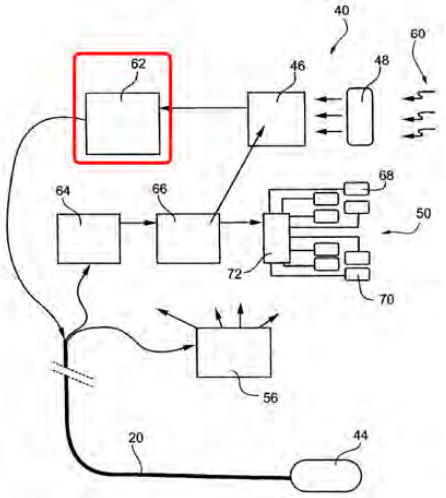
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Adler 940 (Figure 4) ***Alternatively***, this limitation is met if USB is used, rather than LVDS, as a communications medium between the endoscope 10 and processing device 30 as contemplated by the following disclosure. "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		appropriate software for carrying out image processing of the output of the endoscope. The skilled person will appreciate that the wire connection 20 may be an optical connection or may instead use RF or a like means of wireless communication. The miniature endoscopic front-end 10 may be designed for connection to any standard PC input (the USB input for example)." (Adler 940 at 9:24-38 (emphasis added).) A driver would necessarily be required to drive a USB signal over wire connection 20. To the extent this element is not expressly disclosed, it is inherent in Adler 940. Specifically, section 7.1.1 of the USB Specification Revision 1.0 is directed to "USB Driver Characteristics": "The USB uses a differential output driver to drive the USB data signal onto the USB cable. The static output swing of the driver in its low state must be below the VOL of 0.3 V with a 1.5 kW load to 3.6 V and in its high state must be above the VOH of 2.8 V with a 15 kW load to ground as listed in Table 7-4. The output swings between the differential high and low state must be well balanced to minimize signal skew. Slew rate control on the driver is required to minimize the radiated noise and cross talk. The driver's outputs must support three-state operation to achieve bi-directional half duplex operation. High impedance is also required to isolate the port from downstream devices that are being hot inserted or which are connected but powered down. The driver must tolerate a voltage on the signal pins of

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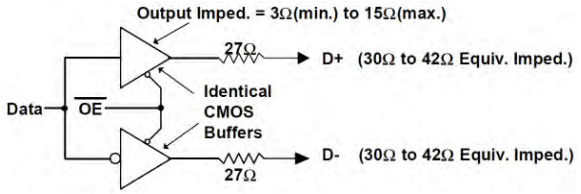
Claims	**Asaida 782**	**in combination with one or more of the following references**
		-0.5 V to 3.8 V with respect to local ground reference without damage. It must tolerate this voltage for 10.0 µs while the driver is active and driving, and tolerate the condition indefinitely when the driver is in its high impedance state." (USB Spec. Rev. 1.0 at 111-13.)  USB Spec. Rev. 1.0 (Figure 7-1) "TIA/EIA-644, otherwise known as LVDS, is a signaling method used for high-speed, low-power transmission of binary data over copper. This signaling technique uses lower output-voltage levels than the 5-V differential standards (such as TIA/EIA-422B) to reduce power consumption, increase switching speed, and allow operation with a 3.3-V supply rail. The LVDS current-mode drivers create a differential voltage (250 mV to 450 mV) across a 100-Ω load. The LVDS receiver detects signals as low as ±100 mV with as much as ±1-V ground noise. The standard specifies a recommended maximum data rate of 655 Mbit/s (and a theoretical maximum of 1.923 Gbit/s on a lossless line)." (TI LVDS at 1.) "The intended application of this signaling technique is for

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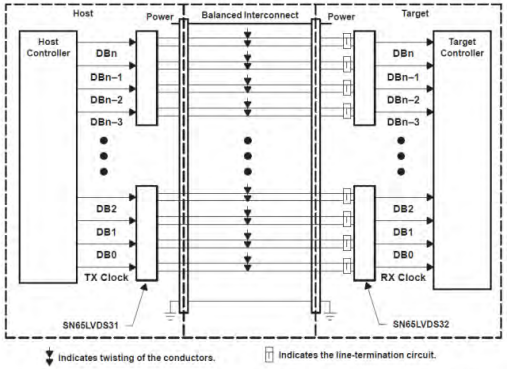
Claims	**Asaida 782**	**in combination with one or more of the following references**
		baseband data transmission over controlled impedance media of approximately 100 Ω, where the transmission media may be printed circuit board (PCB) traces, backplanes, or cables." (TI LVDS at 1.) "Figure 1 shows a typical connection with LVDS drivers and receivers."  Figure 1. Typical Connection With LVDS Drivers and Receivers TI LVDS (Figure 1) "The LVDS driver produces a differential voltage across a 100-Ω load in the range of 247 mV to 454 mV with a typical offset voltage of 1.2 V relative to ground (see Figure 2). Most drivers are commonly imple3mented as current-mode devices, which allow frequency to be virtually independent of power consumption. These two characteristics, low voltage swings and constant current, allow LVDS drivers to operate at higher data rates and lower power dissipation."

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		(TI LVDS at 2.) "As the need for higher bandwidth accelerates, system designers are choosing differential signaling to satisfy high bandwidth requirements while reducing power, increasing noise immunity, and decreasing EMI emissions. LVDS is a low swing, differential signaling technology providing very fast data transmission, common-mode noise rejection, and low power consumption over a broad frequency range. The Virtex-E family delivers the programmable industry's highest bandwidth and most flexible differential signaling solution for direct interfacing to industry-standard LVDS devices." (Virtex-E LVDS at 1.) "With up to 36 I/O pairs operating at 622 Megabits per second (Mb/s) or up to 344 I/O pairs operating at over 311 Mb/s, the Virtex-E family supports multiple 10 Gb/s ports while maintaining high signal integrity with low power consumption. Unlike other PLD solutions, all Virtex-E LVDS I/Os support input, output, and I/O signaling, providing a system designer unparalleled flexibility in board layout." (Virtex-E LVDS at 1.) Advantages of LVDS include: "• LVDS is specified to be technology and process independent. • LVDS is EMI tolerant. Common-mode noise is equally removed by two conductors and rejected by the receiver. • No transmission medium is defined in the standard. The medium can be tailored to meet the specific application

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		requirements. • The typical LVDS voltage swing is 350 mV, resulting in a higher transfer rate and lower power consumption." (Virtex-E LVDS at 2.) "There are two configurations that are used in LVDS applications, point-to-point and multi-drop. The Virtex-E family supports both LVDS configurations. **Point-to-Point** In point-to-point configuration, there is one transmitter and one receiver. The LVDS driver is a current source that drives a differential pair of lines. The typical current drive is 3.5 mA. The receiver has high DC impedance. The majority of the driver current flows across the termination resistor generating about 350 mV at the receiver inputs (Figure 1). **Multi-Drop** A multi-drop LVDS configuration has one transmitter and multiple receivers. The differential termination resistor is placed close to the last receiver (Figure 3)." (Virtex-E LVDS at 2.) Among the many applications that LVDS is suited for are "digital cameras" and "multimedia peripherals." (Virtex-E LVDS at 2-3.) "Figure 1 shows the schematic of a standard LVDS driver driving the Virtex-E receiver. An LVDS driver drives the two 50 W transmission lines into a Virtex-E LVDS receiver.

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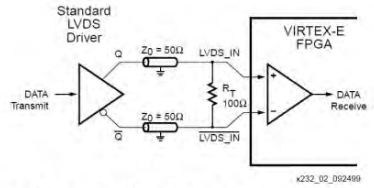
		The two 50 W single-ended transmission lines can be micro-strip, strip-line, a 100 W differential twisted pair, or a similar balanced differential transmission line." (Virtex-E LVDS at 3.)  Figure 1: A Standard LVDS Driver Driving a Virtex-E LVDS Receiver Virtex-E LVDS (Figure 1) "As may be seen, the circuit of FIG. 4 employs a plurality of LVDS circuits 11. Each circuit 11 includes a respective driver 54 and a respective receiver 56. Each driver 54 receives a respective input signal Din0, Din1 . . . Dinn, which are digital logic levels of, for example, 3.3 volts for logic "1" and zero volts for logic "0". Changes in state in these signals are transmitted over the differential lines to the respective receivers 56. Each receiver 56 generates a respective output signal Dout0, Dout1, . . . Doutn, which are at the several hundred millivolt level." (Chung 290 at 2:27-36.)

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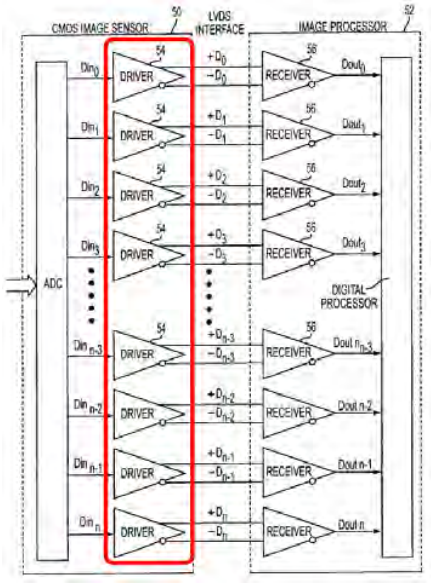
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Chung 290 (Figure 4)
a processor, and	"The signal processing section 8 adds the two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, supplied from the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, for each of the color signals, in such a manner that switching between upper and lower lines on both sides of a center line is done on a field-by-field basis to form interlaced digital three-color signals D_R, D_G and D_B. The signal processing section 8 also processes the digital three color signals D_R, D_G and D_B using, for example, gamma correction and image enhancement." (Asaida 782 at 5:62-6:4.)	"In FIG. 1 and FIG. 2, the circuit configuration of an electronic endoscope according to the embodiment is shown. In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having a number of scanning lines or the like suitable for the scanning line of the NTSC system, and to this CCD 1, a timing generator 16 is connected, and to this timing generator 16, an NTSC crystal oscillator 17, a PAL crystal oscillator 18, and a switching device 19 are provided. Furthermore, a first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU 20,

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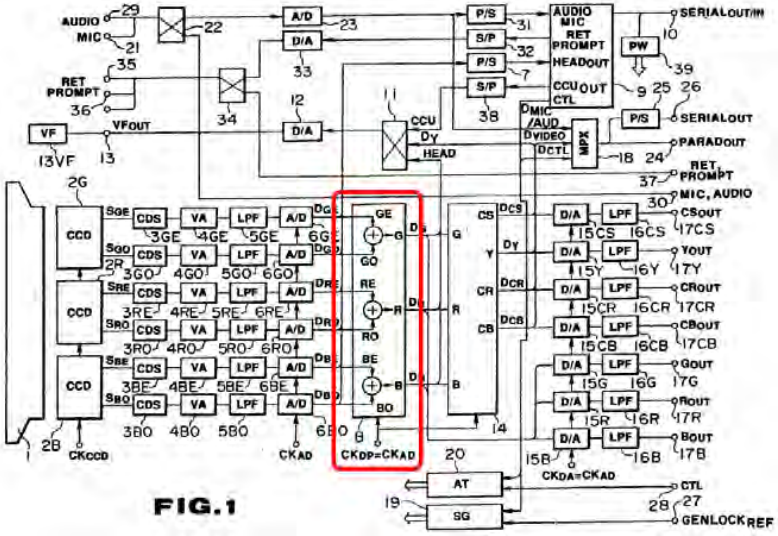
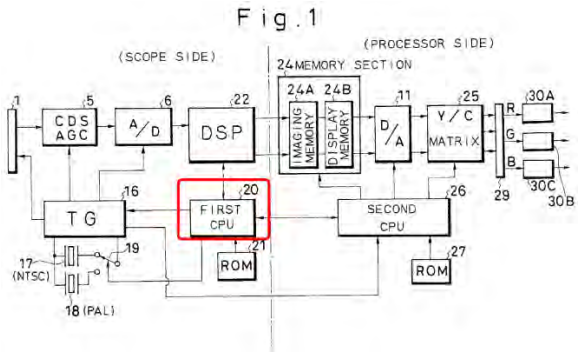
Claims	**Asaida 782**	**in combination with one or more of the following references**
	 FIG.1 Asaida 782 (Figure 1) Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005) (citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)). Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the	either of the oscillators 17, 18 is selected." (Okada 852 at 4:4-15.)  Fig. 1 Okada 852 (Figure 1) "A digital section 30 includes a CCD timing generator 32, a static RAM line store memory 34, a line store timing generator 36, a microprocessor 38, and a USB device interface 40." (Endsley 471 at 3:19-22.) "The USB interface 40, which may be incorporated as part of the microprocessor 38, such as the Intel 82930 microprocessor, reads data from the line store 34." (Endsley 471 at 3:43-46.)

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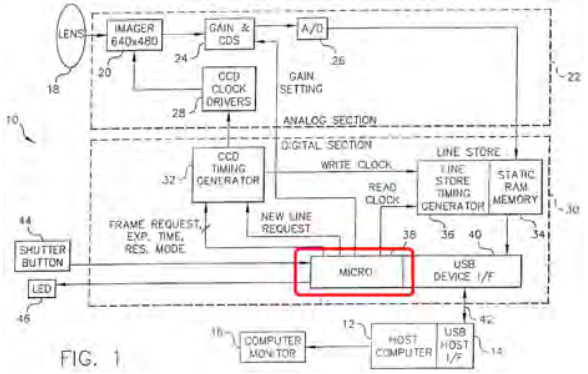
Claims	**Asaida 782**	**in combination with one or more of the following references**
	alleged invention of the '310 patent.	 FIG. 1 Endsley 471 (Figure 1) "A regulator 19, a programmable nonvolatile memory 20, a CPU 21, a selector (SEL) 22, a supply voltage detector 23, a scope switch 24, and a connector 25 are arranged behind the rear end of the insertion unit 11 of the endoscope 2. The regulator 19 converts a CCD driving voltage fed from a CCD driving power supply 18 incorporated in the image processing apparatus 3A into a desired voltage. The programmable nonvolatile memory 20 in which the endoscope-related data is stored is realized with an EEPROM, a flash ROM, an FRAM, or an MRAM." (Oshima 212 at 6:54-63.) "The CPU 21 includes a one-chip microcomputer for performing a plurality of arithmetic operations including communication and writing, or reading. Specifically, the CPU 21 transmits or receives the endoscope-related data to or from the image processing apparatus 3A through a serial

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		interface, and writes or reads the endoscope-related data in or from the nonvolatile memory 20. The CPU 21 includes a ROM, a RAM, a watchdog timer (WDT), a serial controller (S10), a parallel controller (P10), and a counter (CTC). The selector 22 acts as a serial interface means for transmitting or receiving the endoscope-related data over a sole signal line 49. The supply voltage detector 23 detects a fluctuation or drop in supply voltage and outputs a reset signal, thus preventing a malfunction of the CPU 21 or the nonvolatile memory 20." (Oshima 212 at 6:63-7:10.)

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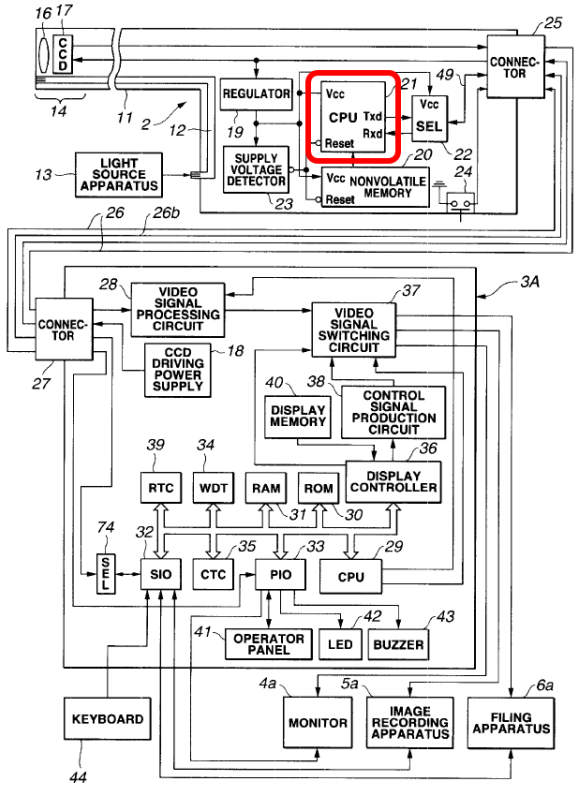
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Oshima 212 (Figure 2)
a memory device, accessible by said processor,	Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005)	"In FIG. 1 and FIG. 2, the circuit configuration of an electronic endoscope according to the embodiment is shown. In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having a number of scanning lines or the like suitable for the scanning line of the

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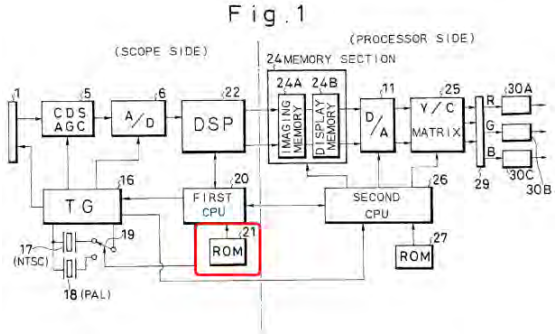
Claims	**Asaida 782**	**in combination with one or more of the following references**
containing camera head information;	(citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)). Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	NTSC system, and to this CCD 1, a timing generator 16 is connected, and to this timing generator 16, an NTSC crystal oscillator 17, a PAL crystal oscillator 18, and a switching device 19 are provided. Furthermore, a first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU 20, either of the oscillators 17, 18 is selected." (Okada 852 at 4:4-15.)  Okada 852 (Figure 1) "The NTSC crystal oscillator 17 generates a signal with a frequency of about 14.32 MHz (N·fh1), and the PAL oscillator 18 on the other side may be an oscillator which generates a signal with the above mentioned frequency of about 17.73 MHz, but in this example, an oscillator which generates a signal with a frequency of N·fh2 [N times the frequency of the horizontal synchronization signal of 15.625 kHz (=fh2)] near the NTSC oscillation frequency is used. Consequently, the change of the circuit member relating to

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		the drive operation, the setting of a constant, or the like become easy. Moreover, to the first CPU 20, a ROM 21 storing setting data for the control meeting the NTSC system or the PAL system is connected." (Okada 852 at 4:16-28 (emphasis added).) "A first example is configured like the above, and in the example, each television system can be selected by selective switches arranged at the processor or the like, and the state of selection of the switches can be grasped by the second CPU 26. Then, this second CPU 26 reads out the setting data of the selected system from the ROM 27 to set the processing contents of each circuit by this setting data. At the same time, the information of the selected system is also transmitted to the first CPU 20 on the scope side from this second CPU 26, and on this scope side, the selected setting data is read out from the ROM 21 by the first CPU 20 to set the processing contents of each circuit, and further, either of the above oscillators 17, 18 is selected and set." (Okada 852 at 4:58-5:3 (emphasis added).) "A digital section 30 includes a CCD timing generator 32, a static RAM line store memory 34, a line store timing generator 36, a microprocessor 38, and a USB device interface 40." (Endsley 471 at 3:19-22.) "The output of the line store memory 34 is connected to the host computer 12 via the USB device interface 40, which operates at a maximum data rate of 12M bits/sec. (See the article 'Universal Serial Bus to Simplify PC I/O', by Michael

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		Slater in Microprocessor Report, Volume 9, Number 5, Apr. 17, 1995 for more detail about the benefits of the USB interface.) The USB interface 40, which may be incorporated as part of the microprocessor 38, such as the Intel 82930 microprocessor, reads data from the line store 34." (Endsley 471 at 3:37-46.) "[T]he present invention includes a novel way of 'line throttle clocking' the image sensor 20 by varying a line blanking interval 68 from line to line, as shown in FIG. 5, so as to transfer lines of data from the CCD image sensor 20 into the line store memory 34 at the appropriate time." (Endsley 471 at 4:54-59.) "FIG.5 shows that, once the image data is transferred by the readout pulse 60 to the light-protected vertical registers 50, the line clocking is 'throttled' to accommodate the storage capacity of the line store memory 34. The line store memory 34 is capable of storing a small number of lines of data and provides block transfer capability at low cost. Whenever the line store memory 34 has sufficient room to accommodate a new line of image data, the timing generator 32 creates the vertical and horizontal timing pulses 62 and 64 needed to read out the next line from the image sensor, as shown in FIG. 5, and then returns to a wait state until sufficient data is transferred from the line store memory 34 to the computer 12 so as to provide room for the next line. Since the waiting period (equal to the line blanking time) depends on the USB bus traffic, the line readout times and frame readout times are variable, rather than fixed, as in prior art cameras." (Endsley

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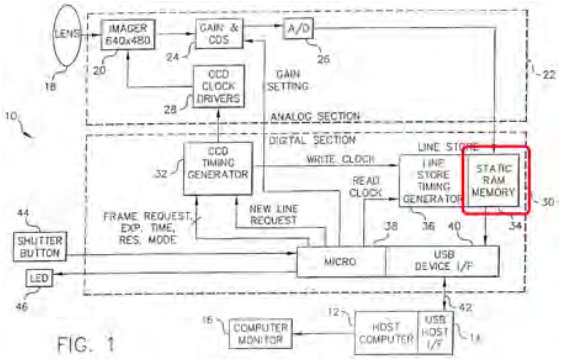
Claims	**Asaida 782**	**in combination with one or more of the following references**
		471 at 4:60-5:9.)  FIG. 1 Endsley 471 (Figure 1) ***Alternatively***, this limitation is met by memory in the USB device interface that contains information related to USB descriptors. "The USB interface 40 . . . may be incorporated as part of the microprocessor 38, such as the Intel 82930 microprocessor." (Endsley 471 at 3:43-45.) "USB devices report their attributes using descriptors. A descriptor is a data structure with a defined format. Each descriptor begins with a byte-wide field that contains the total number of bytes in the descriptor followed by a byte-wide field that identifies the descriptor type. "Using descriptors allows concise storage of the attributes of individual configurations because each configuration may

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		reuse descriptors or portions of descriptors from other configurations that have the same characteristics. In this manner, the descriptors resemble individual data records in a relational database." (USB Spec. Rev. 1.0 at 181.) "A device descriptor describes general information about a USB device. It includes information that applies globally to the device and all of the device's configurations. A USB device has only one device descriptor." (USB Spec. Rev. 1.0 at 182.) "An apparatus sends electrical signals that represent an optical image to a processor for conversion to video signals suitable for display on a display device. The apparatus includes a device for insertion into a region to be viewed for developing an optical image of the region, an imager for generating electrical signals that represent the optical image, and a digital memory for storing information about the imager. The device is adapted to be connected to the processor so that the processor can receive the electrical signals from the imager and obtain information from the digital memory. The processor uses the information from the digital memory in performing the conversion." (Dowdy 082 at Abstract.) "The camera head and endoscope are typically detachable as a unit from the control unit so that a variety of camera heads can be used with a single control unit. This offers a number of advantages. For example, if a first camera head fails, the control unit can be operated with another camera head while

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		the first camera head is being serviced. Also, different types of camera heads, each of which may be most useful for certain procedures, can be used with a single control unit so as to avoid the expense of purchasing and maintaining multiple control units." (Dowdy 082 at 1:25-34 (Background of the Invention).) "In one general aspect, this invention features an apparatus for providing electrical signals that represent an optical image to a processor for conversion to video signals suitable for display on a display device. The apparatus includes a device for insertion into a region to be viewed for developing an optical image of the region, an imager for generating electrical signals that represent the optical image, and a digital memory for storing information about the imager. The device is adapted to be connected to the processor so that the processor can receive the electrical signals from the imager and obtain information from the digital memory. The processor uses the information from the digital memory in performing the conversion." (Dowdy 082 at 1:38-50 (Summary of the Invention).) "The digital memory stores information about the configuration of the imager. This information can include the location of the imager relative to the device. For example, the information identifies whether the imager is located at the distal end or the proximal end of the device. The imager is a charge coupled device. The information identifies an optical format size of the charge coupled device." (Dowdy 082 at 1:53-59.)

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		"The digital memory also stores information about variations in performance characteristics of the imager relative to nominal performance characteristics. When the apparatus includes optics, the information in the digital memory accounts for variations in performance characteristics of the optics relative to nominal performance characteristics. Similarly, when the imager includes a charge coupled device or a cable for connection to the processor, the information accounts for variations in performance characteristics of the charge coupled device or the cable relative to nominal performance characteristics. The information also identifies variations in luminance and color reproduction by the imager." (Dowdy 082 at 1:60-2:5 (Summary of the Invention).) "When the apparatus is designed for application to particular regions, the information identifies characteristics of the region to be viewed by the imager. This allows the processor to optimize the conversion for parameters that are desirable in a particular application." (Dowdy 082 at 2:6-10.) "In one embodiment, the digital memory is a non-volatile storage device, and can be implemented using an EEPROM." (Dowdy 082 at 2:16-17.) "When the information stored in the digital memory identifies the configuration of the device, the processor modifies the conversion based on the configuration. This allows the processor to automatically optimize the

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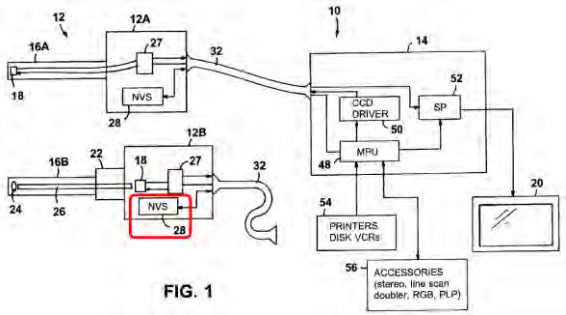
Claims	**Asaida 782**	**in combination with one or more of the following references**
		conversion for different configurations of the device." (Dowdy 082 at 2:34-38.) "Referring also to FIG. 2, to enable different types of camera heads 12 to be used with camera processor 14 without impacting the quality of the video image displayed on video monitor 20, each camera head 12A, 12B (referred to generally with reference numeral 12) includes a non-volatile storage device ("NVS") 28 that stores information identifying the configuration 30 of the particular camera head 12A, 12B. Camera processor 14 uses the information stored in NVS 28 to modify processing of the electrical signals produced by camera head 12, and thereby accounts for the properties of the configuration 30 to which camera head 12 belongs. In a preferred embodiment, NVS 28 is implemented as an electrically erasable programmable read only memory ("EEPROM"). One such EEPROM is an eight pin, 256 byte storage capacity memory available from the Xicor Corp. as model number 24XC02." (Dowdy 082 at 3:62-4:10.)  FIG. 1

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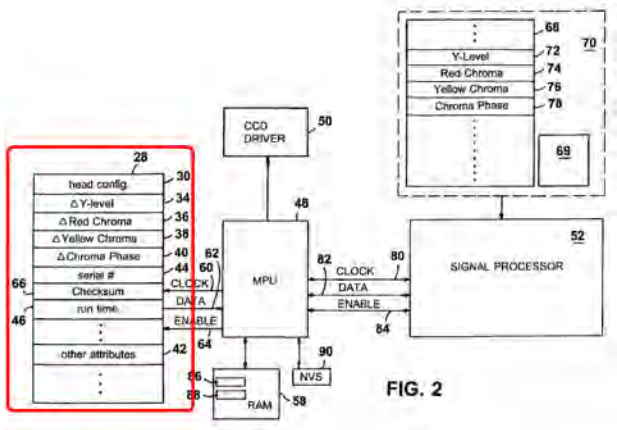
Claims	**Asaida 782**	**in combination with one or more of the following references**
		Dowdy 082 (Figure 1)  Dowdy 082 (Figure 2) "In addition to variations caused by the configuration of camera head 12, the electrical signals produced by camera head 12 can also vary, because performance characteristics of camera heads 12 tend to vary from device to device. These variations, which are caused primarily by differences in optics, CCDs 18, and cables 32 that are attached to camera heads 12 and connect camera heads 12 to camera processor 14, can adversely affect the ability of a camera head 12 to produce electrical signals that result in an optimal video image. Thus, to further ensure consistent performance when different camera heads 12 are used, NVS 28 also stores

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		information that identifies variations in the performance characteristics of a particular camera head 12 from nominal values." (Dowdy 082 at 4:11-24.) "To enable the video image produced at video monitor 20 to be optimized for certain procedures, the NVS 28 of a camera head 12 designed for those procedures can include information 42 that is used by camera processor 14 to optimize certain signal processing attributes. For example, in a camera head 12 designed for procedures requiring improved edge definition, NVS 28 stores edge enhancement information 42 that replaces nominal edge enhancement values stored within and used by camera processor 14. Similarly, in camera heads 12 designed for procedures in which the white or grey brightness ranges are of particular interest, NVS 28 stores information 42 that modifies, respectively, operation of the so-called "knee circuit" (which implements a nonlinear function for compressing, rather than clipping, the upper level, white, component of the video signal) and the operation of the so-called "gamma circuit" (which implements a nonlinear function for optimizing the median level, grey, component of the video signal) implemented by signal processor 14." (Dowdy 082 at 4:36-54.) "For servicing and other purposes, NVS 28 also stores information that identifies the serial number 44 of camera head 12 and a measure 46, in minutes and hours, of the run time that camera head 12 has experienced." (Dowdy 082 at 4:55-58.)

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		"Referring also to FIG. 3, MPU 48 uses the information stored in NVS 28 to control the operation of CCD driver 50 and signal processing circuitry 52. When the user connects cable 32 of camera head 12 to camera processor 14, and, if necessary, powers up video endoscopy system 10, MPU 48 detects the connection and responds by downloading the information from NVS 28 into a memory 58, such as a RAM, of MPU 48 (step 200). MPU 48 reads the stored information out of NVS 28 through a serial data link in cable 32 that includes a CLOCK line 60 controlled by MPU 48 and a DATA line 62 that is shared by NVS 28 and MPU 48." (Dowdy 082 at 5:9-19.) "Referring to FIG. 4, in a more detailed view, camera head 12 includes CCD 18 (located, as discussed, either in the head or at the tip of the endoscope), NVS 28 and a set of button switches 92 for system control, and camera processor 14 includes a camera controller 94 and a signal processor 96. Cable 32, which connects camera head 12 to camera processor 14, carries drive signals from CCD driver 50 in signal processor 96, electrical signals from CCD 18 to a preamplifier 98 in signal processor 96, data between NVS 28 and MPU 48 in camera controller 94, and signals from button switches 92 to MPU 48." (Dowdy 082 at 6:48-58.)

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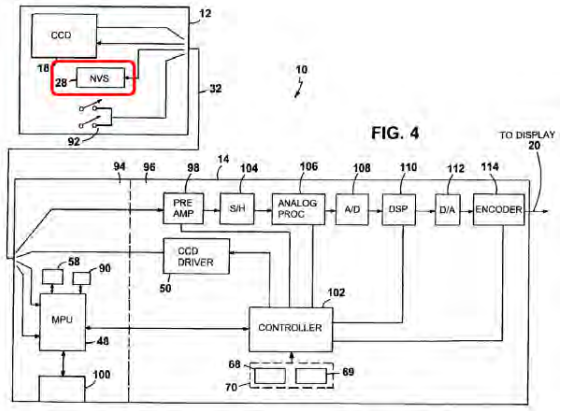
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Dowdy 082 (Figure 4) "MPU 48 controls signal processor 96 in response to signals from button switches 92 and signals from controls in a front panel 100 of camera controller 94. The controls in front panel 100 allow the user of video endoscopy system 10 to configure button switches 92 to perform desired functions. Thus, for example, button switches 92 could be configured to cause signal processor 96 to pause the video image displayed at video monitor 20 (FIG. 1). MPU 48 also displays system parameters at front panel 100, interacts with NVS 28 by downloading information about camera head 12 and updating run time information in NVS 28, updates signal processing parameters in light of the information about camera head 12, and communicates with signal processor 96, all as discussed above." (Dowdy at 6:59-7:5.)

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		"A nonvolatile, programmable memory is incorporated in an endoscope. Endoscope-related data closely relevant to the endoscope, such as, an endoscope model name and the number of power feeds are stored in the nonvolatile memory. The endoscope is connected to an external image processing apparatus, and endoscope-related data is read from the nonvolatile memory. Based on the read endoscope-related data, the use situation of the endoscope is grasped or the endoscope is managed. The number of power feeds is varied depending on the use situation of the endoscope, and written in the nonvolatile memory. Thus, the endoscope-related data is used to maintain the endoscope and reduce a load to be incurred by the external image processing apparatus that is a connected apparatus. Consequently, the endoscope can be managed and maintained easily using a small software system." (Oshima 212 at Abstract.) "[An] object of the present invention is to provide an endoscope system in which endoscope-related data including a use situation of an endoscope can be checked readily." (Oshima 212 at 1:60-62.) "A regulator 19, a programmable nonvolatile memory 20, a CPU 21, a selector (SEL) 22, a supply voltage detector 23, a scope switch 24, and a connector 25 are arranged behind the rear end of the insertion unit 11 of the endoscope 2. The regulator 19 converts a CCD driving voltage fed from a CCD driving power supply 18 incorporated in the image processing apparatus 3A into a desired voltage. The programmable nonvolatile memory 20 in which the

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		endoscope-related data is stored is realized with an EEPROM, a flash ROM, an FRAM, or an MRAM." (Oshima 212 at 6:54-63.) "Especially important data out of endoscope-related data storable in the nonvolatile memory 20 includes, for example, an endoscope model name, the structure of the distal part of an endoscope, a cleaning tube/adaptor name, a CCD model name, a type of optical filter in a CCD, information relating to the channels in an endoscope, information relating to the switches on an endoscope, a version number, and identification data." (Oshima 212 at 29:16-25.)

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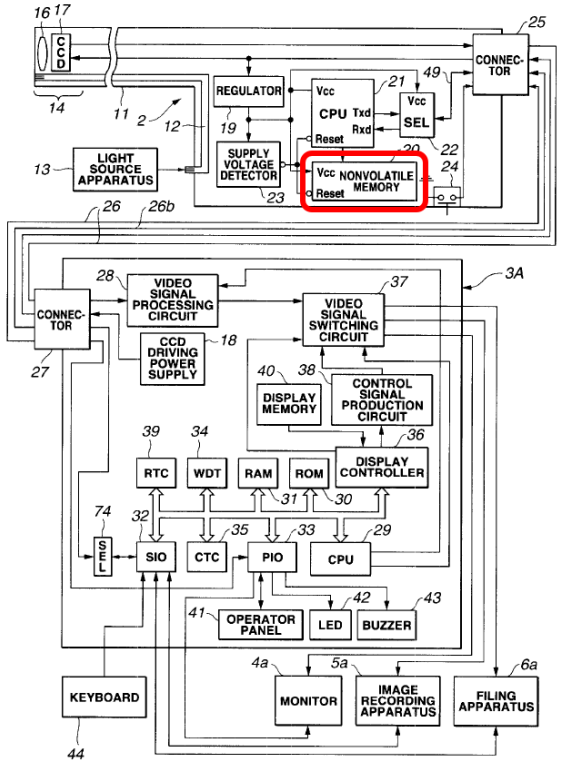
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Oshima 212 (Figure 2) "FIG. 35 describes processing to be performed in the image processing apparatus 3A, which has the ability to communicate with the endoscope 2 and is connected to the endoscope 2, for treating count data contained in data to be stored in the nonvolatile memory 20 in the endoscope 2." (Oshima 212 at 29:59-63.)

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		"The connected apparatus 3A uses connection sensing means (not shown) incorporated in the endoscope and the connected apparatus to judge whether it has been connected to the endoscope 2 (S321). If connection is sensed, identification data or an endoscope model name is read first (S322)." (Oshima 212 at 29:66-30:4.) "From the foregoing description of the prior art, it is clear that the 'bad pixel' data is never transferred to the camera portion, but instead remains in the local controller memory. Accordingly if a camera has been subjected to pixel evaluation for existence of blemishes using a CCU with a blemish compensating capacity as described above, another camera cannot be used in its place with the same CCU unless the CCU blemish compensator is again operated to evaluate the pixels of the new camera. Moreover, assuming that blemish compensation is desired, a camera that has been evaluated by the CCU of Fig. 1 is not interchangeable with another like blemish compensator-equipped CCU unless it is first re-evaluated for blemishes." (Zu 391 at 5-6.) "This non-interchangeability of cameras with a CCU is especially limiting in the case of video endoscopes. During surgery, it may be necessary to employ two or more video endoscopes when only one CCU may be available. With a compensator-equipped CCU as shown in Fig. 1, substitution of one video camera endoscope for another may be frustrated by the need to first evaluate the camera for blemishes and record the 'bad pixels' in the CCU's digital memory so that

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		compensation may be accomplished when video information is acquired by the endoscope's camera." (Zu 391 at 6.) "The object of this invention is to facilitate use of video cameras having known pixel blemishes with different camera control units." (Zu 391 at 6.) "The present invention comprises incorporating into a CCD-type video camera an electronically programmable non-volatile memory which stores the location of 'bad' pixels and is controlled by a device which is located remotely from the camera in a separate CCU. This arrangement assures that video cameras are interchangeable with CCU's regardless of CCD blemish content." (Zu 391 at 6.) "Fig. 2 illustrates the invention. Except as described hereinafter, the system shown in Fig. 2 incorporates the same elements and the same functions as the system of Fig. 1, and identical elements are identified by the same numerals. In this case, the camera 2 is modified by incorporating therein an electronically programmable non-volatile digital memory 42 which is coupled to camera connector 14 via a suitable bus 44." (Zu 391 at 7.)

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		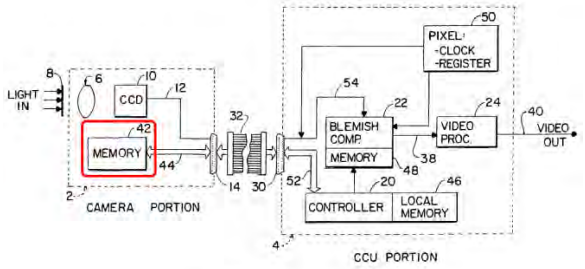 FIG. 2 Zu 391 (Figure 2) "In the operational mode, the data in memory 42 is transferred to memories 46 and 48 whenever the unit is energized. The blemish compensation operation is then performed by the blemish compensator 22 using pixel address data downloaded from camera memory 42. The pixel address data is downloaded from camera memory 42 to blemish compensator memory 48 by the controller 20 via the buses 44 and 52." (Zu 391 at 8.) "When the operational mode is initiated with the camera coupled to a CCU 4 as described, the controller 22 downloads the pixel address data from the camera's memory 42 to the protected local memory 46 of the controller 20. Subsequently that data is loaded into the volatile memory 48 of the blemish compensator 22. Typically this data transfer from camera memory 42 t the local memory 46 of the controller occurs after a forced rest imposed by controller 20, which clears, resets, and reloads all non-protected CCU

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		memory." (Zu 391 at 9.)
said camera control unit having at least one digital serial receiver and	"The camera control unit CCU, constituting part of the video camera according to the present invention, is provided with a serial input/output port 40, as shown in FIG. 3, which is connected to the serial input/output port 10 of the camera head unit by an optical fiber cable, not shown, constituting transmission means." (Asaida 782 at 8:5-10.) To the extent this element is not expressly disclosed, it is inherent in Asaida 782. It would be within the knowledge of one of ordinary skill in the art at the time of the alleged invention that transmitting a serial digital signal over a cable would necessarily require a driver to drive the signal and a receiver to receive the signal. Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005) (citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)). Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	To the extent this element is not expressly disclosed, it is inherent in Endsley 471 by virtue of disclosing and claiming USB as a communications medium. Specifically, section 7.1.2 of the USB Specification Revision 1.0 is directed to "Receiver Characteristics": "A differential input receiver must be used to accept the USB data signal. The receiver must feature an input sensitivity of at least 200 mV when both differential data inputs are in the range of at least 0.8 V to 2.5 V with respect to its local ground reference. This is called the common mode input voltage range. Proper data reception is also required when the differential data lines are outside the common mode range, as shown in Figure 7-4. The receiver must tolerate static input voltages between -0.5 V to 3.8 V with respect to its local ground reference without damage. In addition to the differential receiver, there must be a single-ended receiver for each of the two data lines. The receivers must have a switching threshold between 0.8 V and 2.0 V (TTL inputs). It is recommended that the single-ended receiver have some hysteresis to reduce its sensitivity to noise." (USB Spec. Rev. 1.0 at 113.)

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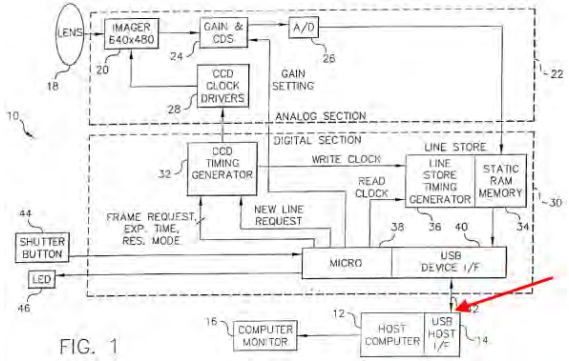
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Endsley 471 (Figure 1) "Reference is now made to FIG. 4, which is an schematic block diagram of the miniature endoscope according to a preferred embodiment of the present invention. Parts that are identical to those shown above are given the same reference numerals and are not referred to again except as necessary for an understanding of the present embodiment. Optical assembly 48 receives light, indicated by arrows 60, from an object being viewed. The light is processed by optical assembly 48, as will be explained below, to reach image sensor 46 were it is converted from photons into electrical signals. The electrical signals are digitized and passed to a transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Adler 940 at 10:7-19 (emphasis added).) If the endoscope uses an LVDS transmitter to drive the data

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		through communication link 20 to the processing device 30, the processing device 30 must necessarily receive the data with a digital serial receiver. ***Alternatively***, this limitation is met if USB is used, rather than LVDS, as a communications medium between the endoscope 10 and processing device 30 as contemplated by the following disclosure. "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope. The skilled person will appreciate that the wire connection 20 may be an optical connection or may instead use RF or a like means of wireless communication. The miniature endoscopic front-end 10 may be designed for connection to any standard PC input (the USB input for example)." (Adler 940 at 9:24-38 (emphasis added).) A receiver would necessarily be required to receive a USB signal over wire connection 20. To the extent this element is not expressly disclosed, it is inherent in Adler 940.

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		Specifically, section 7.1.2 of the USB Specification Revision 1.0 is directed to "Receiver Characteristics": "A differential input receiver must be used to accept the USB data signal. The receiver must feature an input sensitivity of at least 200 mV when both differential data inputs are in the range of at least 0.8 V to 2.5 V with respect to its local ground reference. This is called the common mode input voltage range. Proper data reception is also required when the differential data lines are outside the common mode range, as shown in Figure 7-4. The receiver must tolerate static input voltages between -0.5 V to 3.8 V with respect to its local ground reference without damage. In addition to the differential receiver, there must be a single-ended receiver for each of the two data lines. The receivers must have a switching threshold between 0.8 V and 2.0 V (TTL inputs). It is recommended that the single-ended receiver have some hysteresis to reduce its sensitivity to noise." (USB Spec. Rev. 1.0 at 113.) "Figure 1 shows a typical connection with LVDS drivers and receivers."

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		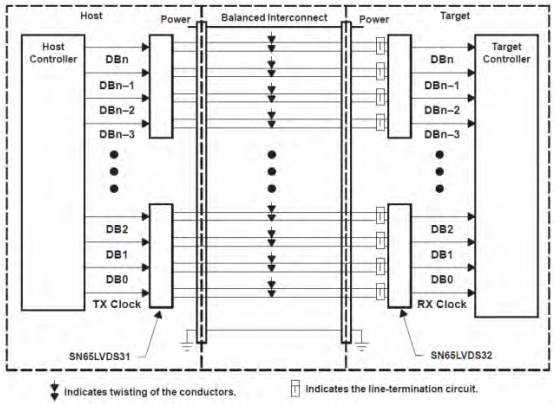 Figure 1. Typical Connection With LVDS Drivers and Receivers TI LVDS (Figure 1) "The recommended voltage applied to the receiver is between ground and 2.4 V with a common mode range of 0.2 V to 2.2 V. The receiver has a sensitivity level of ±100 mV to correctly assume the intended binary state (see Figure 2). The LVDS interconnecting media must be matched with the 100-Ω termination resistor located at the inputs of the receiver." (TI LVDS at 4.) "There are two configurations that are used in LVDS applications, point-to-point and multi-drop. The Virtex-E family supports both LVDS configurations. **Point-to-Point** In point-to-point configuration, there is one transmitter and one receiver. The LVDS driver is a current source that drives

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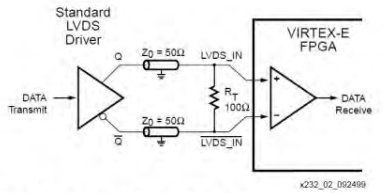
		a differential pair of lines. The typical current drive is 3.5 mA. The receiver has high DC impedance. The majority of the driver current flows across the termination resistor generating about 350 mV at the receiver inputs (Figure 1). **Multi-Drop** A multi-drop LVDS configuration has one transmitter and multiple receivers. The differential termination resistor is placed close to the last receiver (Figure 3)." (Virtex-E LVDS at 2.) Among the many applications that LVDS is suited for are "digital cameras" and "multimedia peripherals." (Virtex-E LVDS at 2-3.) "Figure 1 shows the schematic of a standard LVDS driver driving the Virtex-E receiver. An LVDS driver drives the two 50 W transmission lines into a Virtex-E LVDS receiver. The two 50 W single-ended transmission lines can be micro-strip, strip-line, a 100 W differential twisted pair, or a similar balanced differential transmission line." (Virtex-E LVDS at 3.)  Figure 1: A Standard LVDS Driver Driving a Virtex-E LVDS Receiver

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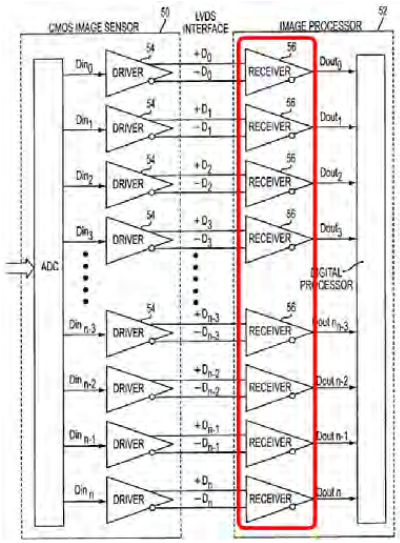
		Virtex-E LVDS (Figure 1) "As may be seen, the circuit of FIG. 4 employs a plurality of LVDS circuits 11. Each circuit 11 includes a respective driver 54 and a respective receiver 56. Each driver 54 receives a respective input signal Din0, Din1 . . . Dinn, which are digital logic levels of, for example, 3.3 volts for logic "1" and zero volts for logic "0". Changes in state in these signals are transmitted over the differential lines to the respective receivers 56. Each receiver 56 generates a respective output signal Dout0, Dout1, . . . Doutn, which are at the several hundred millivolt level." (Chung 290 at 2:27-36.) 

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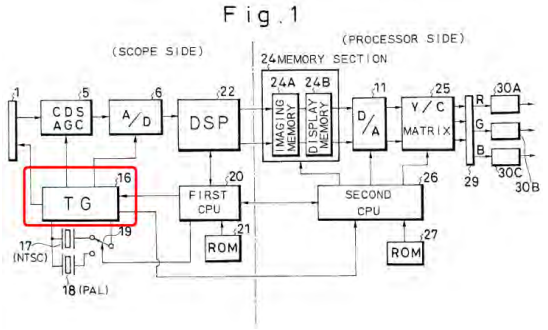
Claims	**Asaida 782**	**in combination with one or more of the following references**
		Chung 290 (Figure 4)
is controlled based at least in part upon said timing signal particular to said camera head;	"[W]ith the present video camera unit, the two-line-concurrent three-color imaging output signals S_{RO}, S_{RE}, S_{GO}, S_{GE}, S_{BO} and S_{BE}, obtained by the solid-state image sensors 2R, 2G, and 2B, are changed by the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE into two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}. The two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, are converted by the P/S converter 7 into serial data as the camera output data $HEAD_{OUT}$, which are serially outputted at the serial input/output port 10 by means of the encoder/decoder 9." (Asaida 782 at 5:50-61.) "[T]he synchronizing circuit block 19 is supplied with a reference synchronizing signal $GENLOCK_{REF}$ for generator locking through synchronizing input terminal 27, while the control circuit block 20 is supplied with a control signal CTL through a control input terminal 28." (Asaida 782 at 7:16-21.) "The encoder/decoder 9 encodes the serial data supplied from P/S converters 7 and 31 and serially transmits the encoded serial data via the serial input/output port 10 to a camera control unit CCU described below, while also decoding various serial data transmitted from the camera control unit CCU to the serial input/output port 10, such as return video signals D_{RET}, prompter signals D_{PROMPT}, output signals CCU_{OUT} from the camera control unit CCU or control data D_{CTL}." (Asaida 782 at 7:35-43.)	"In FIG. 1 and FIG. 2, the circuit configuration of an electronic endoscope according to the embodiment is shown. In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having a number of scanning lines or the like suitable for the scanning line of the NTSC system, and to this CCD 1, a timing generator 16 is connected, and to this timing generator 16, an NTSC crystal oscillator 17, a PAL crystal oscillator 18, and a switching device 19 are provided. Furthermore, a first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU 20, either of the oscillators 17, 18 is selected." (Okada 852 at 4:4-15.) Fig. 1  Okada 852 (Figure 1)

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	Thus, encoder/decoder 9 transmits either a separate timing signal or a timing signal embedded in the serial data signal received from P/S converter 7 (which originated from image sensors 2R, 2G, and 2B) and sent to the CCU through input/output port 10. The CCU is controlled based at least in part upon the timing signal.	"A first example is configured like the above, and in the example, each television system can be selected by selective switches arranged at the processor or the like, and the state of selection of the switches can be grasped by the second CPU 26. Then, this second CPU 26 reads out the setting data of the selected system from the ROM 27 to set the processing contents of each circuit by this setting data. At the same time, the information of the selected system is also transmitted to the first CPU 20 on the scope side from this second CPU 26, and on this scope side, the selected setting data is read out from the ROM 21 by the first CPU 20 to set the processing contents of each circuit, and further, either of the above oscillators 17, 18 is selected and set." (Okada 852 at 4:58-5:3.) "That is, if the NTSC system is selected, the NTSC system oscillator 17 is connected to the timing generator 16 by the switching circuit 19. In this timing generator 16, the oscillating signal with, for example, a frequency of 14.32 MHz generated in the oscillator 17 is divided to form the horizontal synchronization signal with a frequency of 15.734 kHz (fh1) and the vertical synchronization signal with a frequency of 59.94 Hz, and the driving pulse based on this is given to the CCD 1. Then, the picture signal extracted from this CCD 1 is subjected to the digital conversion after passing through the AGC circuit 5 for performing the correlative double sampling and the amplification processing, and as shown in FIG. 2, this digital picture signal is subjected to a specified processing by the DSP circuit 22, and it is supplied to the memory section 24 on the processor

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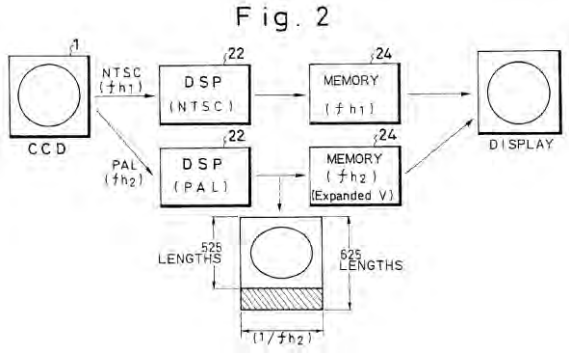
		side." (Okada 852 at 5:4-20.)  Okada 852 (Figure 2) "In this memory section 24, the picture data is written in the imaging memory 24A in the timing of the synchronization signal formed in the timing generator 16, and after that, this picture data is read out in the same timing to be stored in the display memory 24B (as the data corresponding to the number of scanning lines of 525). The data of this display memory 24 is converted into the signals of R, G, and B from the brightness signal and the color difference signal in the Y/C matrix circuit 25 after being converted to the analog signal in the D/A converter 11. Then, each of these signals of R, G, and B is outputted to a monitor of the NTSC system through the isolation device 29 and the buffers 30 (A to C), and consequently, a picture of the NTSC system is displayed on the monitor." (Okada 852 at 5:21-35 (emphasis added).)

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		Thus, the CCU is controlled at least in part based upon said timing signal. "The output of the line store memory 34 is connected to the host computer 12 via the USB device interface 40, which operates at a maximum data rate of 12M bits/sec." (Endsley 471 at 3:37-39.) "[T]he present invention includes a novel way of 'line throttle clocking' the image sensor 20 by varying a line blanking interval 68 from line to line, as shown in FIG. 5, so as to transfer lines of data from the CCD image sensor 20 into the line store memory 34 at the appropriate time." (Endsley 471 at 4:54-59.) "FIG.5 shows that, once the image data is transferred by the readout pulse 60 to the light-protected vertical registers 50, the line clocking is 'throttled' to accommodate the storage capacity of the line store memory 34. The line store memory 34 is capable of storing a small number of lines of data and provides block transfer capability at low cost. Whenever the line store memory 34 has sufficient room to accommodate a new line of image data, the timing generator 32 creates the vertical and horizontal timing pulses 62 and 64 needed to read out the next line from the image sensor, as shown in FIG. 5, and then returns to a wait state until sufficient data is transferred from the line store memory 34 to the computer 12 so as to provide room for the next line. Since the waiting period (equal to the line blanking time) depends on the USB bus traffic, the line readout times and frame readout times are

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		variable, rather than fixed, as in prior art cameras." (Endsley 471 at 4:60-5:9.) The USB Device 40 transmits either a separate timing signal (*see, e.g.*, Section 5.10.2 of USB Spec. Rev. 1.0) or a timing signal embedded in the serial data signal sent to the CCU. The CCU is controlled based at least in part upon the timing signal.
wherein a plurality of camera heads, each with differing timing signals, are attachable to and controlled by said camera control unit.	Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005) (citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)). Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	"The camera 10 includes an optical section 18 for imaging light from a subject upon an electronic image sensor 20. A preferred image sensor is a Kodak KAI-0320CM interline transfer, progressive-scan charge-coupled-device (CCD) image sensor with a usable active image area having 640 columns and 480 rows of color photoelements arranged in the well-known Bayer color filter array pattern (see U.S. Pat. No. 3,971,065 for a description of the Bayer pattern)." (Endsley 613 at 3:24-31.) "An analog section 22 in the camera 10 includes the sensor 20, a CDS/gain block 24 for performing correlated double sampling (CDS) and setting the analog gain, an analog-to-digital (A/D) converter 26 for converting the analog output signal from the CCD sensor 20 to, e.g., an 8-bit digital signal, and CCD clock drivers 28 for clocking the sensor 20." (Endsley 613 at 3:31-37.)

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		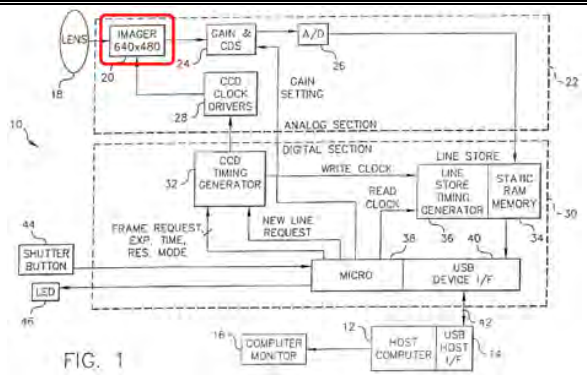 FIG. 1 Endsley 613 (Figure 1) The camera control unit disclosed and claimed in Endsley 471 is host computer 12, which is a general purpose computer that is attachable to a plurality of camera heads via USB cable 42. Indeed, "[t]he goal [of the USB specification] is to enable such devices from different vendors to inter-operate in an open architecture. The specification is intended as an enhancement to the PC architecture spanning portable, business desktops, and home environments. It is intended that the specification allow system OEMs and peripheral developers adequate room for product versatility and market differentiation without the burden of carrying obsolete interfaces or losing compatibility." (USB Spec. Rev. 1.0 at 11.) "The advantage of this invention is that once blemishes are

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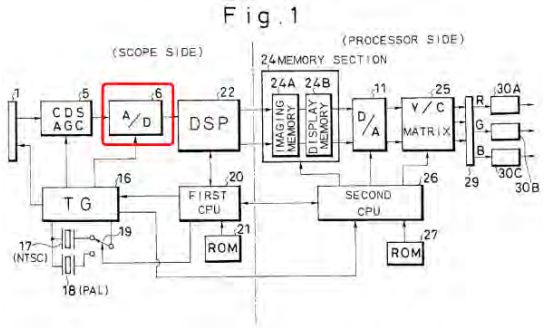
		located, this information is translated to the non-volatile memory in the camera so that it is accessible by any CCU to which the camera is attached." (Zu 391 at 10.)
10. The video imaging system according to claim 9 wherein said camera head produces analog image data, said camera head further comprising a converter, for converting an analog image signal to a digital image signal.	*See* Claim 9. The analysis of Claim 9 is incorporated by reference in its entirety. "The two-line-concurrent three-color imaging output signals S_{RO}, S_{RE}, S_{GO}, S_{GE}, S_{BO} and S_{BE}, processed for level adjustment by the level adjustment circuits 4RO, 4RE, 4GO, 4GE, 4BO and 4BE, are transmitted by means of low-pass filters 5RO, 5RE, 5GO, 5GE, 5BO and 5BE, respectively, to A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, functioning as analog/ digital converting means, respectively." (Asaida 782 at 5:14-22.) "A driving clock CK_{AD} having a frequency four times the frequency of the color subcarrier frequency f_{SC}, or $4f_{SC}$, is supplied to the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, by means of a timing generator, not shown. The A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE digitize the two-line-concurrent three-color imaging output signals S_{RO}, S_{RE}, S_{GO}, S_{GE}, S_{BO} and S_{BE} with the $4f_{sc}$ driving clock CK_{AD} to produce two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, respectively. The two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, produced by the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, are supplied to a parallel/serial converter (P/S converter) 7 and to a signal processing section 8." (Asaida 782 at 5:23-37.)	"[T]o the CCD 1, an AGC (automatic gain control) circuit including a CDS (correlative double sampling) circuit is connected similarly to that in the prior art, and to this AGC circuit 5, a DSP (digital signal processor) circuit 22 is connected through an A/D converter 6." (Okada 852 at 4:29-33.)  Okada 852 (Figure 1) "The camera 10 includes an optical section 18 for imaging light from a subject upon an electronic image sensor 20. A preferred image sensor is a Kodak KAI-0320CM interline transfer, progressive-scan charge-coupled-device (CCD) image sensor with a usable active image area having 640 columns and 480 rows of color photoelements arranged in the well-known Bayer color filter array pattern (see U.S. Pat. No. 3,971,065 for a description of the Bayer pattern)."

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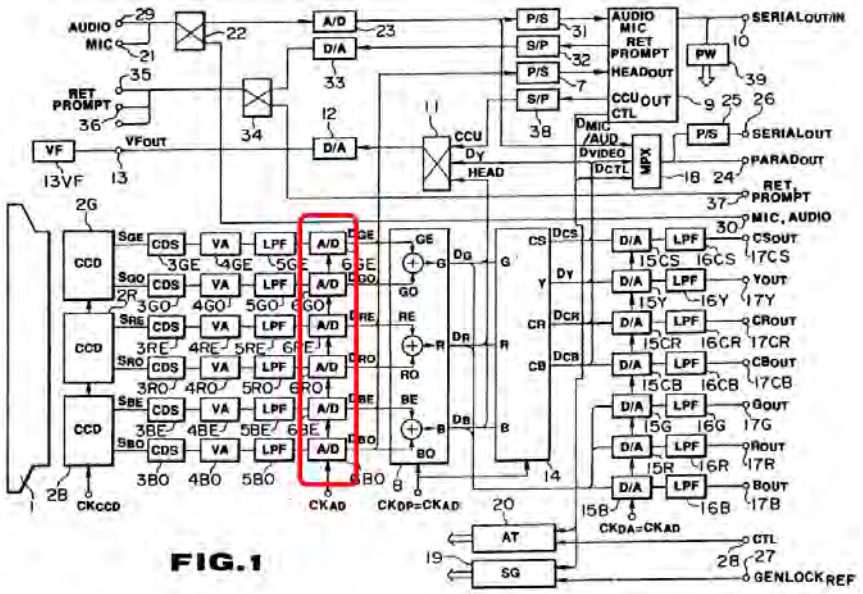
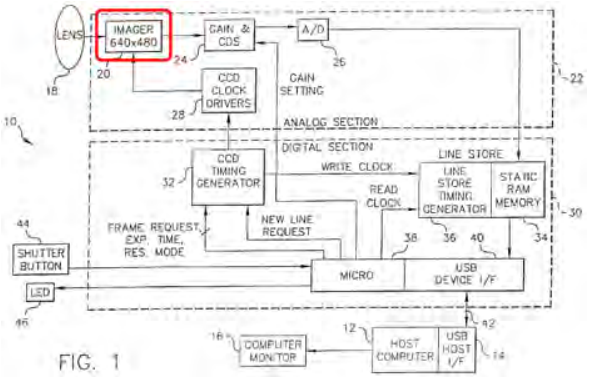
Claims	**Asaida 782**	**in combination with one or more of the following references**
	 FIG.1 Asaida 782 (Figure 1)	(Endsley 613 at 3:24-31.) "An analog section 22 in the camera 10 includes the sensor 20, a CDS/gain block 24 for performing correlated double sampling (CDS) and setting the analog gain, an analog-to-digital (A/D) converter 26 for converting the analog output signal from the CCD sensor 20 to, e.g., an 8-bit digital signal, and CCD clock drivers 28 for clocking the sensor 20." (Endsley 613 at 3:31-37.)  FIG. 1 Endsley 613 (Figure 1) "An analog section 22 in the camera 10 includes the sensor 20, a CDS/gain block 24 for performing correlated double sampling (CDS) and setting the analog gain, an analog-to-digital (A/D) converter 26 for converting the analog output signal from the CCD sensor 20 to, e.g., an 8-bit digital signal, and CCD clock drivers 28 for clocking the sensor 20."

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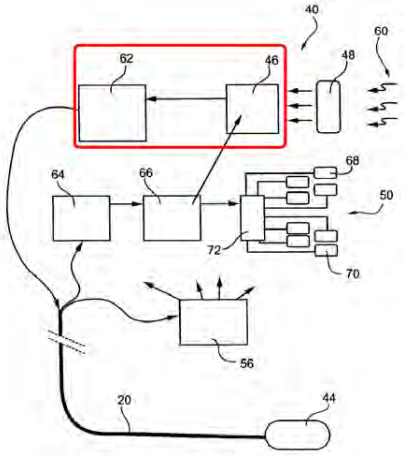
Claims	**Asaida 782**	**in combination with one or more of the following references**
		(Endsley 471 at 3:13-18.) "Reference is now made to FIG. 4, which is an schematic block diagram of the miniature endoscope according to a preferred embodiment of the present invention. Parts that are identical to those shown above are given the same reference numerals and are not referred to again except as necessary for an understanding of the present embodiment. Optical assembly 48 receives light, indicated by arrows 60, from an object being viewed. The light is processed by optical assembly 48, as will be explained below, to reach image sensor 46 were it is converted from photons into electrical signals. The electrical signals are digitized and passed to a transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Adler 940 at 10:7-19 (emphasis added).) 

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		Adler 940 (Figure 4) Because "the electrical signals are digitized and passed to a transmitting device 62" in the camera head, the camera head must contain a converter for converting an analog stream of video data into a stream of digital video data. "One of the advantages of CMOS image sensors (CMOS imagers) over CCD imagers is that the CMOS imager chip can include digital signal processing circuitry. In practice, the signal processing is more often performed on a companion chip, in order to provide greater application flexibility. However, CMOS imagers often have integrated analog to digital converters to convert the analog signal to a digital bit stream that can be processed by the companion chip. The digitized information then must be transferred to companion chip or other external devices for picture storage, processing, or transmission." (Chung 290 at 1:17-27 (emphasis added).) "FIG. 4 illustrates CMOS video imaging sensing circuitry according to the preferred embodiment disclosed in co-pending U.S. application Ser. No 09/062,343. This circuitry includes a CMOS image sensor chip 50 and an image processor chip 52. The CMOS image sensor chip 50 typically includes a number of light responsive CMOS pixel sensors which develop analog signals representative of an image. These analog signals are then A to D converted by the ADC circuit to form digital signals Din0, Din1 . . . Dinn. The

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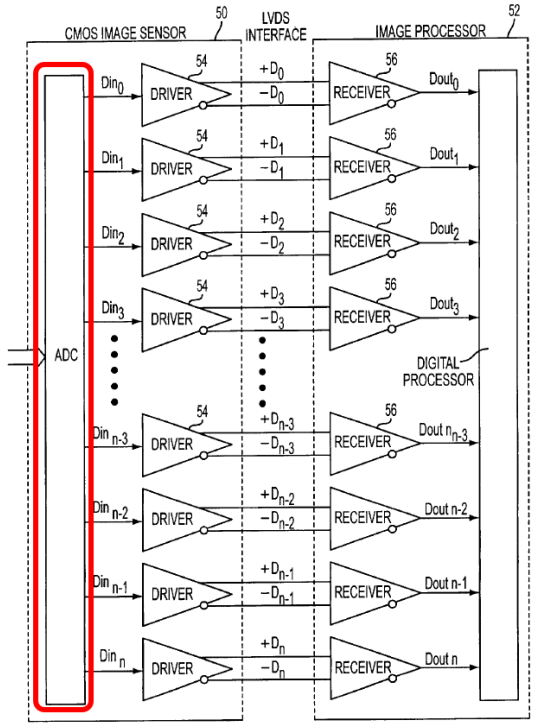
Claims	**Asaida 782**	**in combination with one or more of the following references**
		image processor chip 52 includes a data processor 53 which performs various manipulations of the image data such as compression and color processing. The processor 53 may be software driven or a hardware embodiment." (Chung 290 at 2:14-26.)  Chung 290 (Figure 4)

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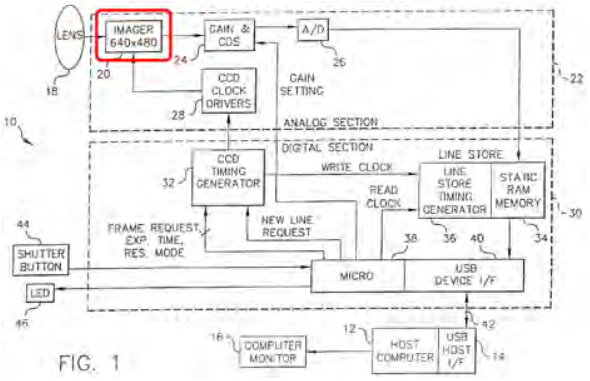
Claims	**Asaida 782**	**in combination with one or more of the following references**
11. The video imaging system according to claim 9 wherein said camera head further comprises a multiplexer, for generating a multiplexed signal, which includes the image signal and control signals.	*See* Claim 9. The analysis of Claim 9 is incorporated by reference in its entirety. "The multiplexor 18 is supplied with control data D_{CTL} from a synchronizing circuit block 19 and a control circuit block 20, while being supplied with voice data D_{MIC}, from a microphone signal inputted from a microphone input terminal 21 by means of a selector 22 and digitized by an A/D converter 23 into audio data $D_{MIC/AUDIO}$. The multiplexor 18 adds the signals D_{CTL} and $D_{MIC/AUDIO}$ to a digital video signal D_{VIDEO} composed of the digital component Video signals D_Y, D_{CR} and D_{CB} or the digital composite video signal D_{CS} supplied from the encoder 14. Output data D_{MPX} from the multiplexor 18, that is, the digital video signal D_{VIDEO} added to the control data D_{CTL} and the audio data $D_{MIC/AUDIO}$, are outputted in parallel at a parallel output port 24, while being converted by P/S converter 25 from parallel data into serial data which are serially outputted at a serial output port 26." (Asaida 782 at 6:67-7:15.)	"The camera 10 includes an optical section 18 for imaging light from a subject upon an electronic image sensor 20. A preferred image sensor is a Kodak KAI-0320CM interline transfer, progressive-scan charge-coupled-device (CCD) image sensor with a usable active image area having 640 columns and 480 rows of color photoelements arranged in the well-known Bayer color filter array pattern (see U.S. Pat. No. 3,971,065 for a description of the Bayer pattern)." (Endsley 613 at 3:24-31.) "An analog section 22 in the camera 10 includes the sensor 20, a CDS/gain block 24 for performing correlated double sampling (CDS) and setting the analog gain, an analog-to-digital (A/D) converter 26 for converting the analog output signal from the CCD sensor 20 to, e.g., an 8-bit digital signal, and CCD clock drivers 28 for clocking the sensor 20." (Endsley 613 at 3:31-37.)  FIG. 1

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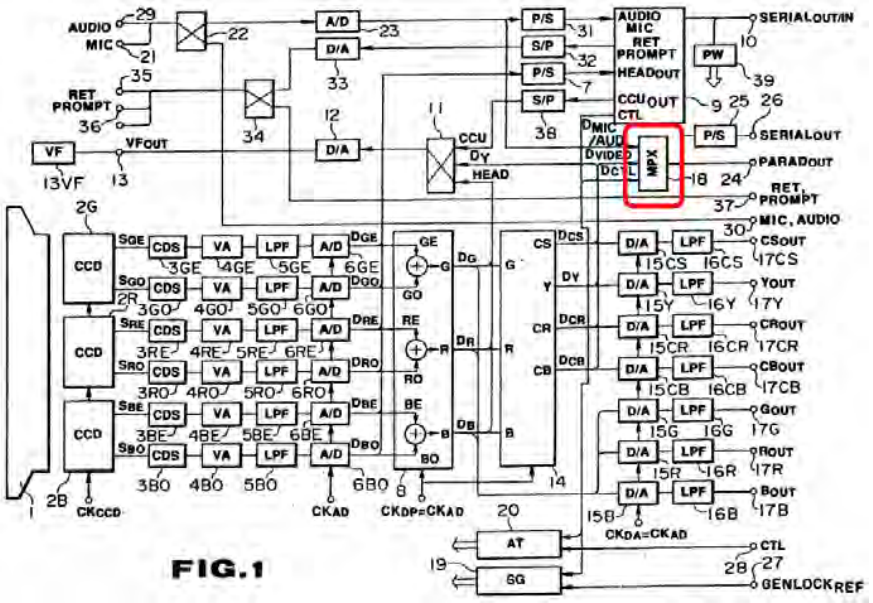
Claims	**Asaida 782**	**in combination with one or more of the following references**
	 Asaida 782 (Figure 1)	Endsley 613 (Figure 1)
12. The video imaging system according to claim 9 wherein said camera head further comprises a	*See* Claim 9. The analysis of Claim 9 is incorporated by reference in its entirety. "A driving clock CK_{AD} having a frequency four times the frequency of the color subcarrier frequency f_{SC}, or $4f_{SC}$, is supplied to the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, by means of a timing generator, not shown. The A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE digitize the two-line-concurrent three-color imaging output signals S_{RO}, S_{RE}, S_{GO}, S_{GE}, S_{BO} and S_{BE} with the $4f_{sc}$ driving clock CK_{AD} to produce two-line-concurrent digital three-color	"The camera 10 includes an optical section 18 for imaging light from a subject upon an electronic image sensor 20. A preferred image sensor is a Kodak KAI-0320CM interline transfer, progressive-scan charge-coupled-device (CCD) image sensor with a usable active image area having 640 columns and 480 rows of color photoelements arranged in the well-known Bayer color filter array pattern (see U.S. Pat. No. 3,971,065 for a description of the Bayer pattern)." (Endsley 613 at 3:24-31.)

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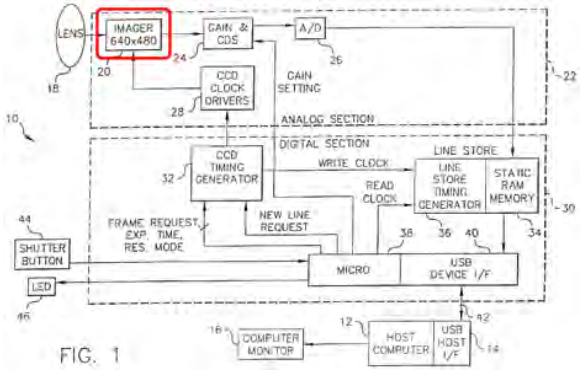
Claims	**Asaida 782**	**in combination with one or more of the following references**
serializer, for serializing the image signal.	signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, respectively. The two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, produced by the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, are supplied to a parallel/serial converter (P/S converter) 7 and to a signal processing section 8." (Asaida 782 at 5:23-37.) "The P/S converter 7 changes the two-line-concurrent digital three color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, supplied from the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO, and 6BE, from parallel data into serial data. The serial data, produced by the P/S converter 7, are supplied as camera output data $HEAD_{OUT}$ to a light-transmitting encoder/decoder 9." (Asaida 782 at 5:38-44.) "The encoder/decoder 9 encodes the serial data, that is, the camera output data $HEAD_{OUT}$, supplied from the P/S converter 7, and outputs the encoded data at a serial input/output port 10 over an optical fiber cable, not shown." (Asaida 782 at 5:45-49.)	"An analog section 22 in the camera 10 includes the sensor 20, a CDS/gain block 24 for performing correlated double sampling (CDS) and setting the analog gain, an analog-to-digital (A/D) converter 26 for converting the analog output signal from the CCD sensor 20 to, e.g., an 8-bit digital signal, and CCD clock drivers 28 for clocking the sensor 20." (Endsley 613 at 3:31-37.)  Endsley 613 (Figure 1) To the extent this element is not expressly disclosed, it is inherent in Endsley 471 by virtue of disclosing and claiming USB as a communications medium. Specifically, section 10.2.2 of the USB Specification Revision 1.0 (Jan. 15, 1996) explains that "[t]he actual transmission of data across the physical USB takes place as a serial bit stream. A Serial Interface Engine (SIE), whether implemented as part of the host or a USB device, handles the

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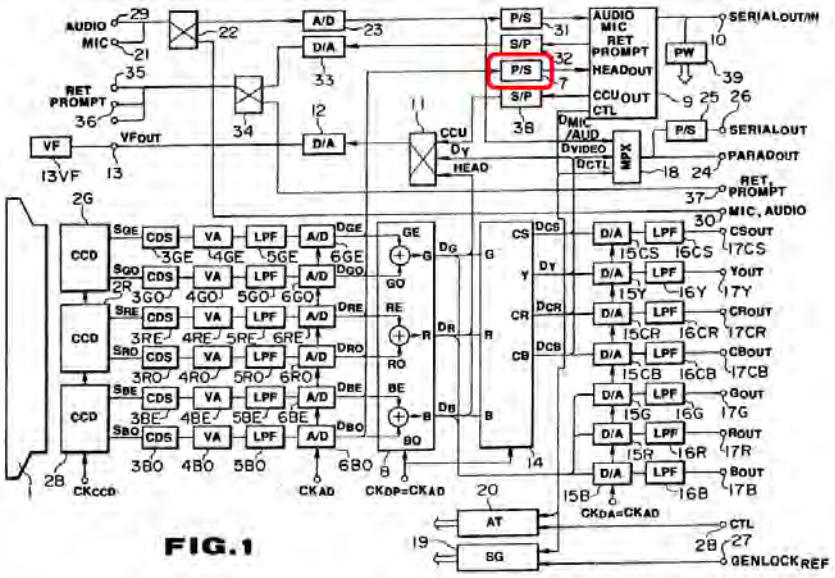
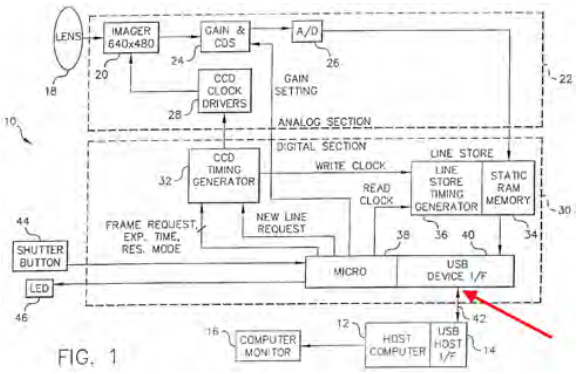
Claims	**Asaida 782**	**in combination with one or more of the following references**
	 FIG.1 Asaida 782 (Figure 1)	serialization and deserialization of USB transmissions. On the host, this SIE is part of the host controller." (USB Spec. Rev. 1.0 at 200.) Thus, in order for USB to be implemented as disclosed and claimed in Endsley 471, there must be "a serializer, for serializing the stream of digital video data for transmission over said cable."  FIG. 1 Endsley 471 (Figure 1) "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		appropriate software for carrying out image processing of the output of the endoscope. The skilled person will appreciate that the wire connection 20 may be an optical connection or may instead use RF or a like means of wireless communication. The miniature endoscopic front-end 10 may be designed for connection to any standard PC input (the USB input for example)." (Adler 940 at 9:24-38 (emphasis added).) "Reference is now made to FIG. 4, which is an schematic block diagram of the miniature endoscope according to a preferred embodiment of the present invention. Parts that are identical to those shown above are given the same reference numerals and are not referred to again except as necessary for an understanding of the present embodiment. Optical assembly 48 receives light, indicated by arrows 60, from an object being viewed. The light is processed by optical assembly 48, as will be explained below, to reach image sensor 46 were it is converted from photons into electrical signals. The electrical signals are digitized and passed to a transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Adler 940 at 10:7-19 (emphasis added).) Because both USB and LVDS are contemplated by Adler 940 as a means for transmitting the stream of digital video data over cable 20, both of which are serial communication protocols, the camera head must include a component that a serializes the digital video data.

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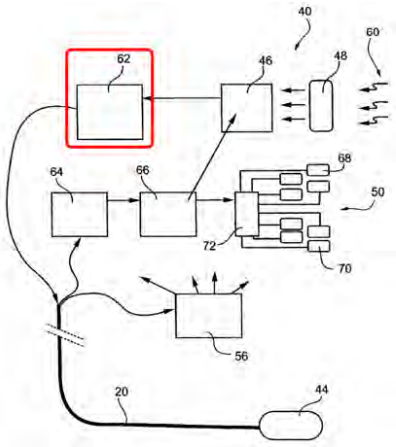
Claims	**Asaida 782**	**in combination with one or more of the following references**
13. The video imaging system according to claim 9 wherein said at least one digital serial driver utilizes Low-Voltage Differential Signals.	*See* Claim 9. The analysis of Claim 9 is incorporated by reference in its entirety. Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005) (citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)). Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	"Reference is now made to FIG. 4, which is an schematic block diagram of the miniature endoscope according to a preferred embodiment of the present invention. Parts that are identical to those shown above are given the same reference numerals and are not referred to again except as necessary for an understanding of the present embodiment. Optical assembly 48 receives light, indicated by arrows 60, from an object being viewed. The light is processed by optical assembly 48, as will be explained below, to reach image sensor 46 were it is converted from photons into electrical signals. The electrical signals are digitized and passed to a transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Adler 940 at 10:7-19.)  Adler 940 (Figure 4)

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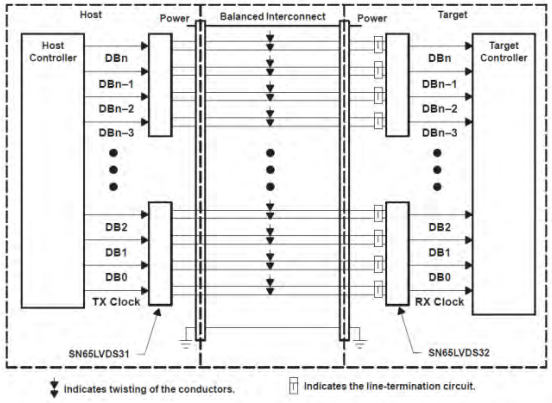
Claims	**Asaida 782**	**in combination with one or more of the following references**
		"Figure 1 shows a typical connection with LVDS drivers and receivers."  Figure 1. Typical Connection With LVDS Drivers and Receivers TI LVDS (Figure 1) "The LVDS driver produces a differential voltage across a 100-Ω load in the range of 247 mV to 454 mV with a typical offset voltage of 1.2 V relative to ground (see Figure 2). Most drivers are commonly imple3mented as current-mode devices, which allow frequency to be virtually independent of power consumption. These two characteristics, low voltage swings and constant current, allow LVDS drivers to operate at higher data rates and lower power dissipation." (TI LVDS at 2.) "Figure 1 shows the schematic of a standard LVDS driver driving the Virtex-E receiver. An LVDS driver drives the

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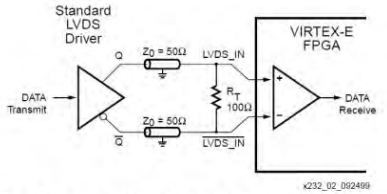
Claims	**Asaida 782**	**in combination with one or more of the following references**
		two 50 W transmission lines into a Virtex-E LVDS receiver. The two 50 W single-ended transmission lines can be micro-strip, strip-line, a 100 W differential twisted pair, or a similar balanced differential transmission line." (Virtex-E LVDS at 3.)  **Figure 1: A Standard LVDS Driver Driving a Virtex-E LVDS Receiver** Virtex-E LVDS (Figure 1) "As may be seen, the circuit of FIG. 4 employs a plurality of LVDS circuits 11. Each circuit 11 includes a respective driver 54 and a respective receiver 56. Each driver 54 receives a respective input signal Din0, Din1 . . . Dinn, which are digital logic levels of, for example, 3.3 volts for logic "1" and zero volts for logic "0". Changes in state in these signals are transmitted over the differential lines to the respective receivers 56. Each receiver 56 generates a respective output signal Dout0, Dout1, . . . Doutn, which are at the several hundred millivolt level." (Chung 290 at 2:27-36.)

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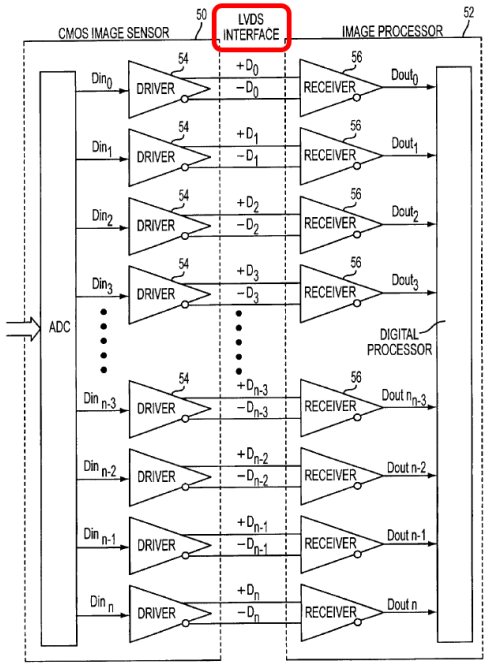
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Chung 290 (Figure 4)
14. The video imaging system according to claim 9 wherein said at least one	*See* Claim 9. The analysis of Claim 9 is incorporated by reference in its entirety. Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005)	"Reference is now made to FIG. 4, which is an schematic block diagram of the miniature endoscope according to a preferred embodiment of the present invention. Parts that are identical to those shown above are given the same reference numerals and are not referred to again except as necessary for an understanding of the present embodiment. Optical assembly 48 receives light, indicated by arrows 60, from an object being viewed. The light is processed by optical

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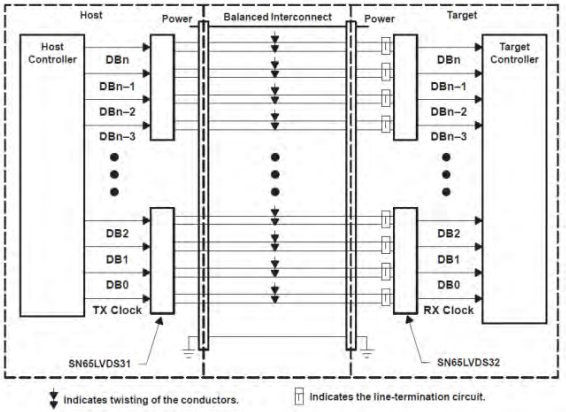
Claims	**Asaida 782**	**in combination with one or more of the following references**
digital serial receiver utilizes Low-Voltage Differential Signals.	(citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)). Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	assembly 48, as will be explained below, to reach image sensor 46 were it is converted from photons into electrical signals. The electrical signals are digitized and passed to a transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Adler 940 at 10:7-19.) If the electrical signals are transmitted to the processing device 30 using an LVDS transmitter, the at least one digital serial receiver in the processing device that receives the signals must necessarily utilize Low-Voltage Differential Signals. "Figure 1 shows a typical connection with LVDS drivers and receivers."  Figure 1. Typical Connection With LVDS Drivers and Receivers

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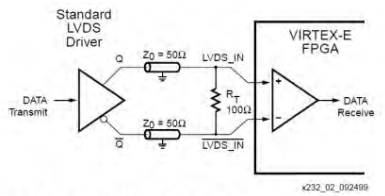
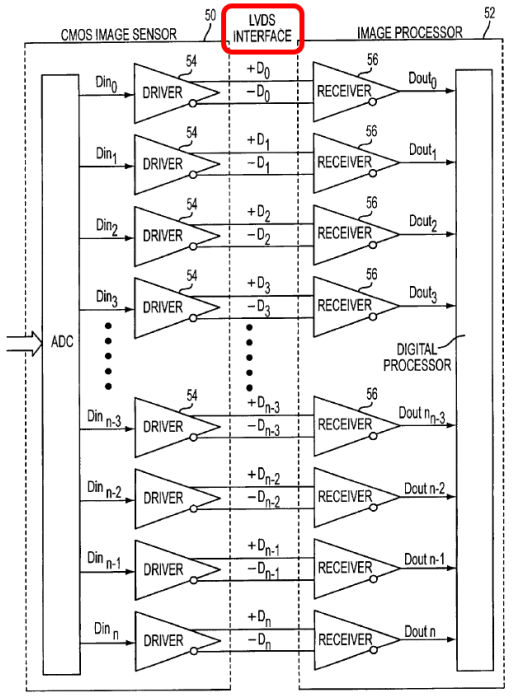
Claims	**Asaida 782**	**in combination with one or more of the following references**
		TI LVDS (Figure 1) "The recommended voltage applied to the receiver is between ground and 2.4 V with a common mode range of 0.2 V to 2.2 V. The receiver has a sensitivity level of ±100 mV to correctly assume the intended binary state (see Figure 2). The LVDS interconnecting media must be matched with the 100-Ω termination resistor located at the inputs of the receiver." (TI LVDS at 4.) "Figure 1 shows the schematic of a standard LVDS driver driving the Virtex-E receiver. An LVDS driver drives the two 50 W transmission lines into a Virtex-E LVDS receiver. The two 50 W single-ended transmission lines can be micro-strip, strip-line, a 100 W differential twisted pair, or a similar balanced differential transmission line." (Virtex-E LVDS at 3.)  **Figure 1: A Standard LVDS Driver Driving a Virtex-E LVDS Receiver** Virtex-E LVDS (Figure 1) "As may be seen, the circuit of FIG. 4 employs a plurality of LVDS circuits 11. Each circuit 11 includes a respective

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		driver 54 and a respective receiver 56. Each driver 54 receives a respective input signal Din0, Din1 . . . Dinn, which are digital logic levels of, for example, 3.3 volts for logic "1" and zero volts for logic "0". Changes in state in these signals are transmitted over the differential lines to the respective receivers 56. Each receiver 56 generates a respective output signal Dout0, Dout1, . . . Doutn, which are at the several hundred millivolt level." (Chung 290 at 2:27-36.) 

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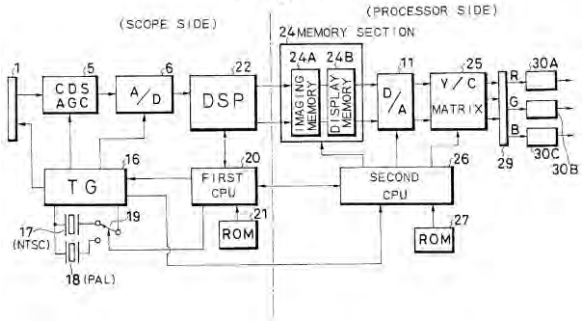
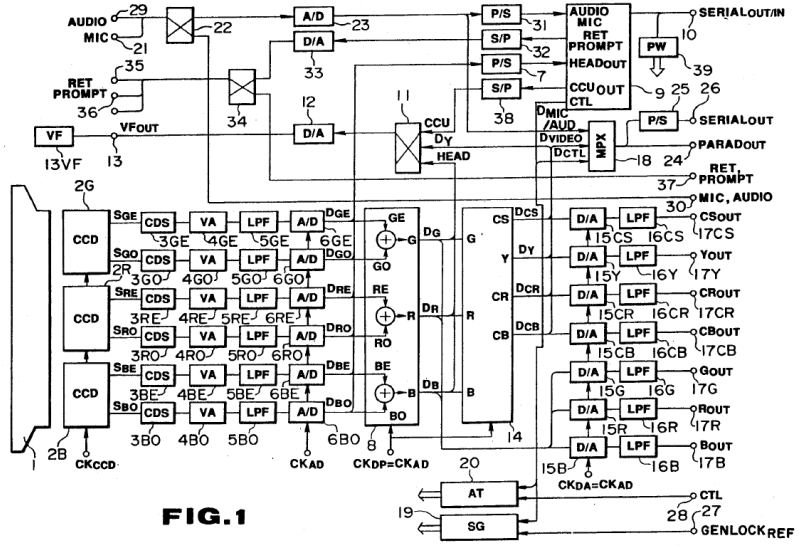
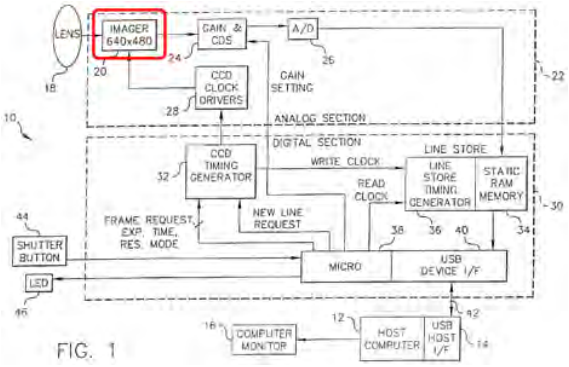
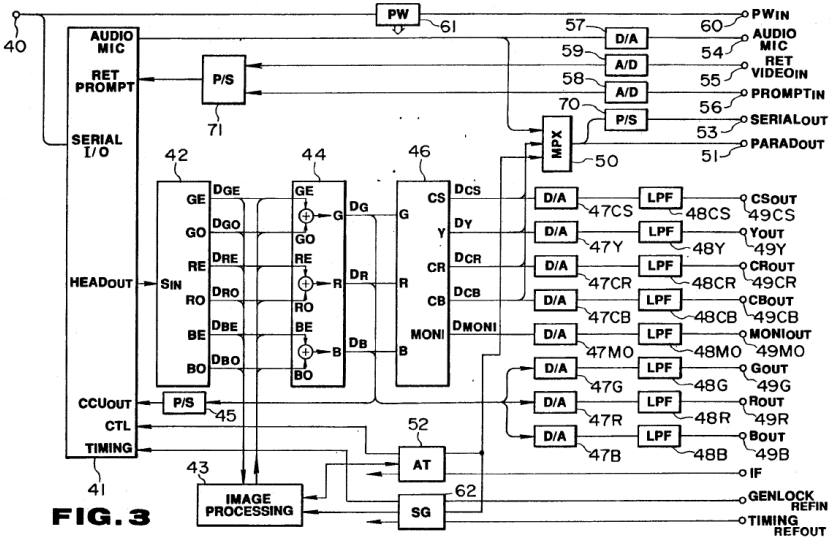
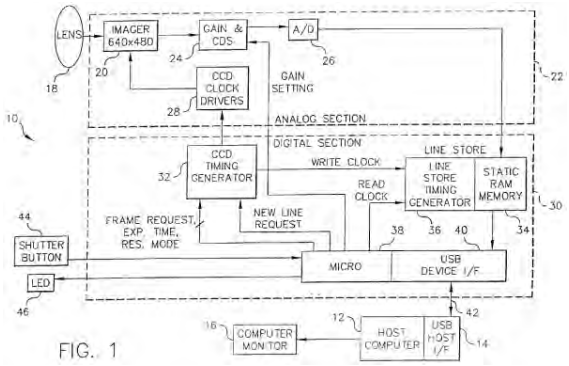
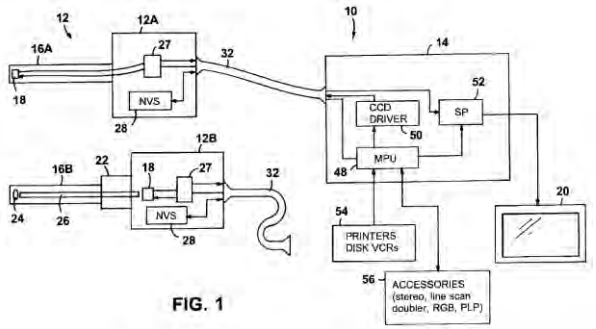
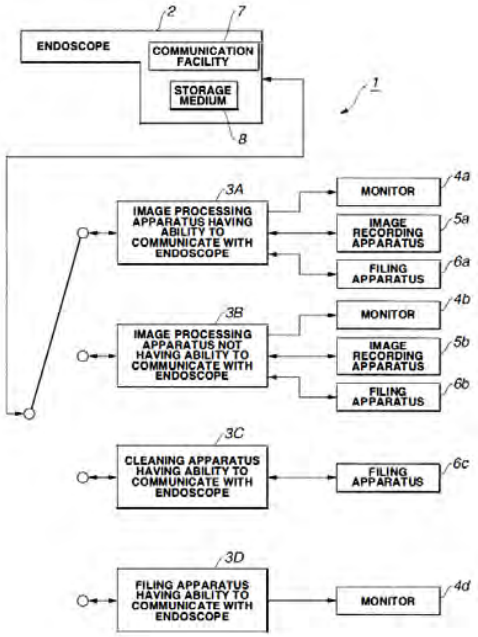
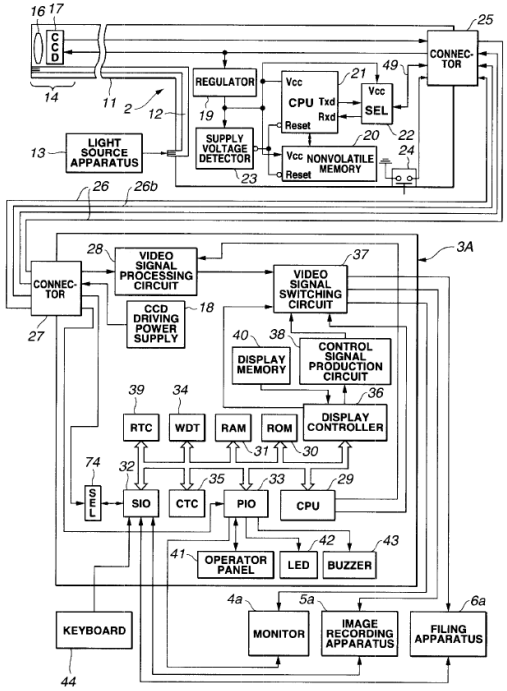
Claims	**Asaida 782**	**in combination with one or more of the following references**
		Chung 290 (Figure 4)
15. A video imaging system comprising:	To the extent the preamble is limiting, Asaida 782 discloses "[a] video imaging system." "This invention relates to a video camera forming digital signals representing an object projected on an imaging device and, more particularly, to a video camera having a signal processing circuit for performing digital signal processing on output signals of the imaging device." (Asaida 782 at 1:7-12.) "FIG. 1 is a block diagram showing an embodiment of a camera head unit of a video camera according to the present invention." (Asaida 782 at 3:44-46.)	To the extent the preamble is limiting, Okada 852 discloses "[a] video imaging system." "The present invention relates to an imaging device for an endoscope, and more particularly, it relates to the composition of an endoscope system which can display a picture imaged by using one scope, by either system selected from the NTSC system and the PAL system." (Okada 852 at 1:12-16." "FIG. 1 is a block diagram showing the circuit configuration of an electronic endoscope equipped with both the NTSC system and the PAL system according to an embodiment of the present invention." (Okada 852 at 3:58-61.) Fig. 1  Okada 852 (Figure 1)

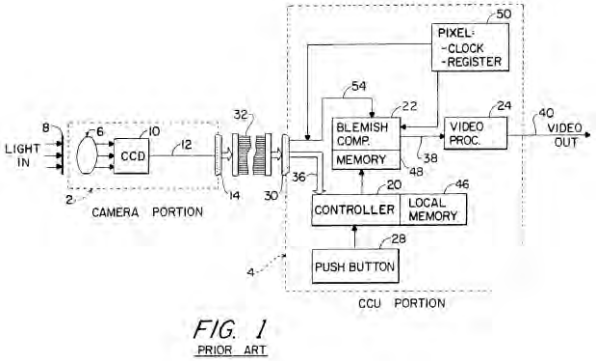
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
	 FIG.1 Asaida 782 (Figure 1) "FIG. 3 is a block diagram showing an embodiment of a camera control unit of the video camera shown in FIG. 1." (Asaida 782 at 3:50-52.)	"The camera 10 includes an optical section 18 for imaging light from a subject upon an electronic image sensor 20. A preferred image sensor is a Kodak KAI-0320CM interline transfer, progressive-scan charge-coupled-device (CCD) image sensor with a usable active image area having 640 columns and 480 rows of color photoelements arranged in the well-known Bayer color filter array pattern (see U.S. Pat. No. 3,971,065 for a description of the Bayer pattern)." (Endsley 613 at 3:24-31.) "An analog section 22 in the camera 10 includes the sensor 20, a CDS/gain block 24 for performing correlated double sampling (CDS) and setting the analog gain, an analog-to-digital (A/D) converter 26 for converting the analog output signal from the CCD sensor 20 to, e.g., an 8-bit digital signal, and CCD clock drivers 28 for clocking the sensor 20." (Endsley 613 at 3:31-37.)  FIG. 1 Endsley 613 (Figure 1)

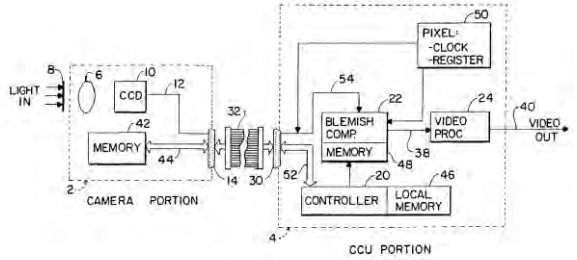
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
	 FIG. 3 Asaida 782 (Figure 3)	To the extent the preamble is limiting, Endsley 471 discloses a video imaging system. Specifically, "[a] block diagram of a digital imaging system according to the invention is shown in FIG. 1. The system includes a camera 10 connected to a host computer 12 via a USB (universal serial bus) cable 42 connected to a USB digital host interface 14, which also provides power to the camera 10. . . . The camera 10 can acquire both still and motion images." (Endsley 471 at 2:49-59.)  FIG. 1 Endsley 471 (Figure 1) To the extent the preamble is limiting, Dowdy 082 discloses "[a] video imaging system." "The invention relates to camera heads for use with remote video display systems such as video endoscopy systems,

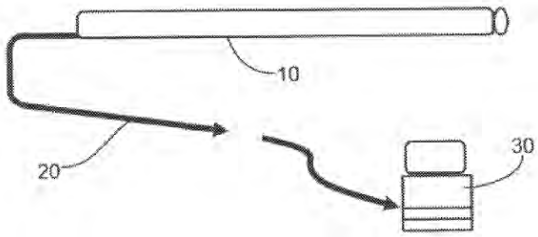
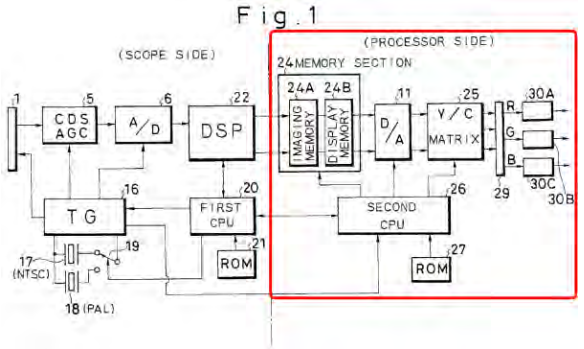
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		borescopes, and other devices." (Dowdy 082 at 1:10-12.) "Referring to FIG. 1, a video endoscopy or borescope system 10 includes a camera head 12 and a camera processor 14. Camera head 12 includes an endoscope 16 for insertion into a region such as a body cavity, and an imaging device, such as a CCD 18, that produces electrical signals representative of an optical image at the distal end of endoscope 16. Camera processor 14 processes the electrical signals produced by camera head 12 to generate a video image that is displayed on a video monitor 20." (Dowdy 082 at 3:24-32.)  FIG. 1 Dowdy 082 (Figure 1) To the extent the preamble is limiting, Oshima 212 discloses "[a] video imaging system. "An endoscope system 1 in accordance with the first embodiment of the present invention shown in FIG. 1

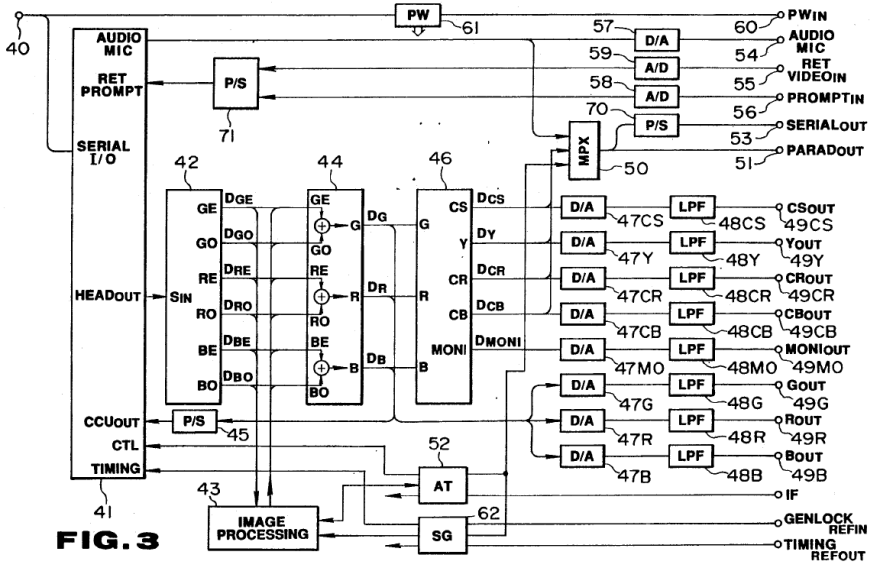
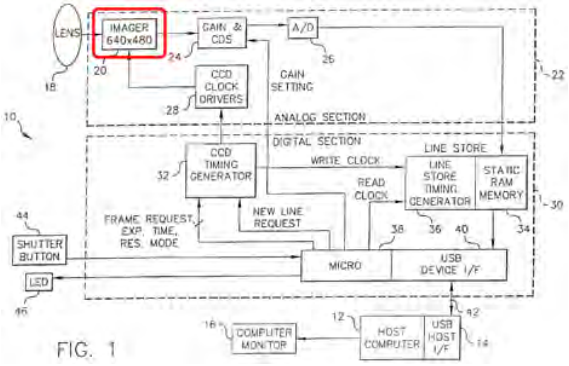
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		consists broadly of an endoscope 2, and connected apparatuses (or peripheral equipment) to be selectively connected to the endoscope. The connected apparatuses include an image processing apparatus 3A, an image processing apparatus 3B, a cleaning apparatus 3C, a filing apparatus 3D, a monitor 4 a, an image recording apparatus 5 a, a filing apparatus 6 a, a monitor 4 b, an image recording apparatus 5 b, a filing apparatus 6 b, a filing apparatus 6 c, and a monitor 4 d. The image processing apparatus 3A has the ability to communicate with the endoscope 2. . . ." (Oshima 212 at 5:15-26.) 

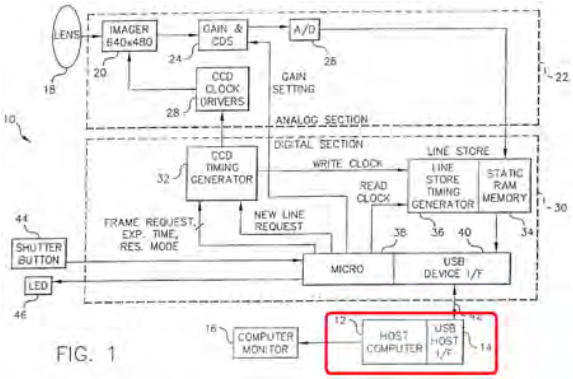
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		Oshima 212 (Figure 1) "FIG. 2 is a block diagram showing in detail the endoscope 2 and the image processing apparatus 3A having the communicating ability which are employed in the present embodiment." (Oshima 212 at 6:34-37.)  Oshima 212 (Figure 2)

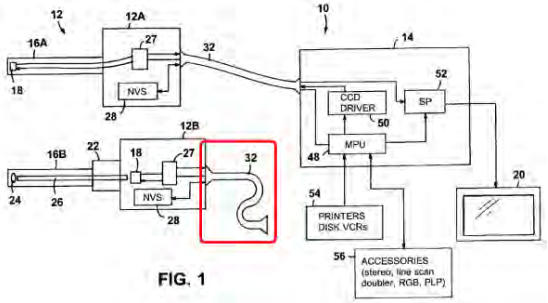
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		To the extent the preamble is limiting, Zu 391 discloses "[a] video imaging system." "This invention relates to compensating for CCD blemishes in video cameras and ore particularly to cameras that are designed to be used interchangeably with camera control units, notably but not exclusively video cameras that are incorporated in endoscopes for use with medical imaging systems." (Zu 391 at 1.) "Fig. 2 illustrates the invention. Except as described hereinafter, the system shown in Fig. 2 incorporates the same elements and the same functions as the system of Fig. 1, and identical elements are identified by the same numerals." (Zu 391 at 7.)  FIG. 1 PRIOR ART Zu 391 (Figure 1)

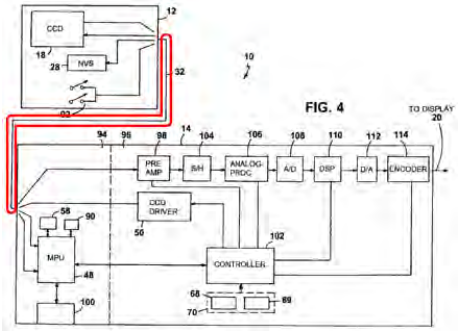
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 FIG. 2 Zu 391 (Figure 2) To the extent the preamble is limiting, Adler 940 discloses "[a] video imaging system." "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope. The skilled person will appreciate that the wire connection 20 may be an optical connection or may instead use RF or a like means of wireless communication. The miniature endoscopic front-end 10 may be designed for connection to any standard PC input (the USB input for example)." (Adler 940 at 9:24-38.)

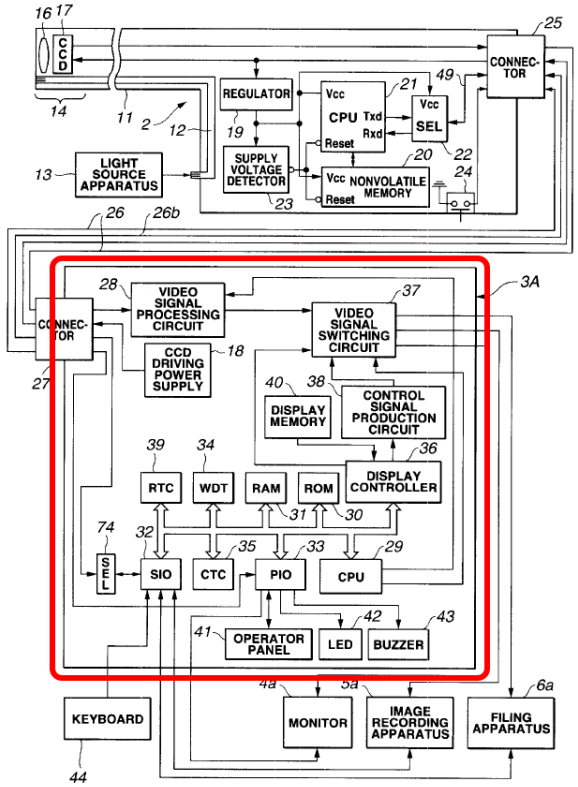
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Adler 940 (Figure 1)
a camera control unit processing a continuous stream of digital video data;	"FIG. 3 is a block diagram showing an embodiment of a camera control unit of the video camera shown in FIG. 1." (Asaida 782 at 3:50-52.) "The video camera according to the present invention is constituted by the above mentioned camera head unit shown in FIG. 1 and the camera control unit CCU arranged and constituted as shown in FIG. 3." (Asaida 782 at 8:1-4.) "The camera control unit CCU, constituting part of the video camera according to the present invention, is provided with a serial input/output port 40, as shown in FIG. 3, which is connected to the serial input/output port 10 of the camera head unit by an optical fiber cable, not shown, constituting transmission means." (Asaida 782 at 8:5-10.)	"[O]n the external processor side, a memory section 24 equipped with an imaging memory 24A and a display memory 24B, a D/A converter 11, a brightness/color signal (Y/C) matrix circuit 25, a second CPU 26 for controlling these circuits, and a ROM 27 storing the setting data for the control meeting the selected television system of the NTSC or the PAL are provided." (Okada 852 at 4:34-40.) 

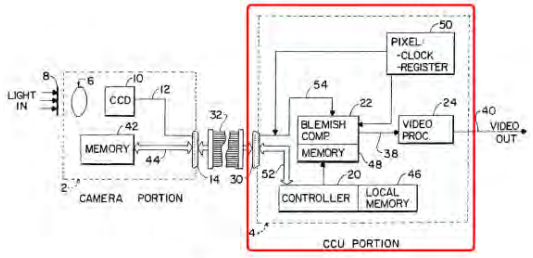
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
	 FIG. 3 Asaida 782 (Figure 3)	Okada 852 (Figure 1) "The camera 10 includes an optical section 18 for imaging light from a subject upon an electronic image sensor 20. A preferred image sensor is a Kodak KAI-0320CM interline transfer, progressive-scan charge-coupled-device (CCD) image sensor with a usable active image area having 640 columns and 480 rows of color photoelements arranged in the well-known Bayer color filter array pattern (see U.S. Pat. No. 3,971,065 for a description of the Bayer pattern)." (Endsley 613 at 3:24-31.) "An analog section 22 in the camera 10 includes the sensor 20, a CDS/gain block 24 for performing correlated double sampling (CDS) and setting the analog gain, an analog-to-digital (A/D) converter 26 for converting the analog output signal from the CCD sensor 20 to, e.g., an 8-bit digital signal, and CCD clock drivers 28 for clocking the sensor 20." (Endsley 613 at 3:31-37.)  FIG. 1	

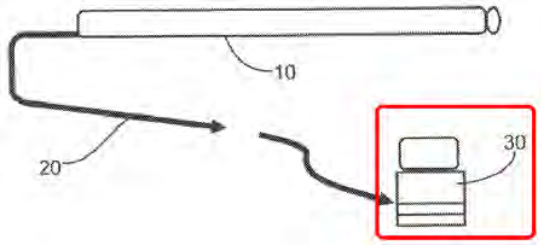
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		Endsley 613 (Figure 1) "The system includes a camera 10 connected to a host computer 12 via a USB (universal serial bus) cable 42 connected to a USB digital host interface 14, which also provides power to the camera 10. . . . The camera 10 can acquire both still and motion images. The camera data is processed by the host computer 12 to create final images that can be displayed on a computer monitor 16, e.g., transmitted along with audio as part of a 'computer videoconference', etc." (Endsley 471 at 2:50-63.) "The host computer 12 controls the camera operation. It can instruct the camera 10 when to take still or motion pictures, and set the electronic exposure time via the CCD timing generator 32, and set the analog gain in the CDS/gain block 24 from the microprocessor 38." (Endsley 471 at 3:54-58.)  FIG. 1

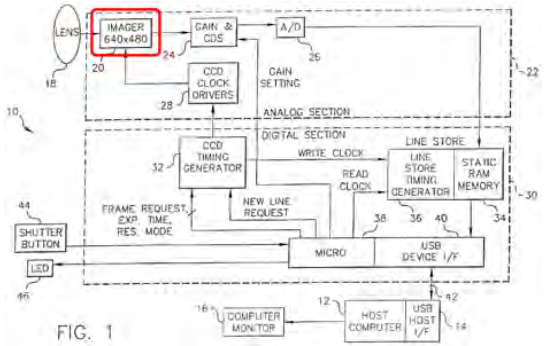
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		Endsley 471 (Figure 1) "Referring to FIG. 4, in a more detailed view, camera head 12 includes CCD 18 (located, as discussed, either in the head or at the tip of the endoscope), NVS 28 and a set of button switches 92 for system control, and camera processor 14 includes a camera controller 94 and a signal processor 96. Cable 32, which connects camera head 12 to camera processor 14, carries drive signals from CCD driver 50 in signal processor 96, electrical signals from CCD 18 to a preamplifier 98 in signal processor 96, data between NVS 28 and MPU 48 in camera controller 94, and signals from button switches 92 to MPU 48." (Dowdy 082 at 6:48-58.)  Dowdy 082 (Figure 1)

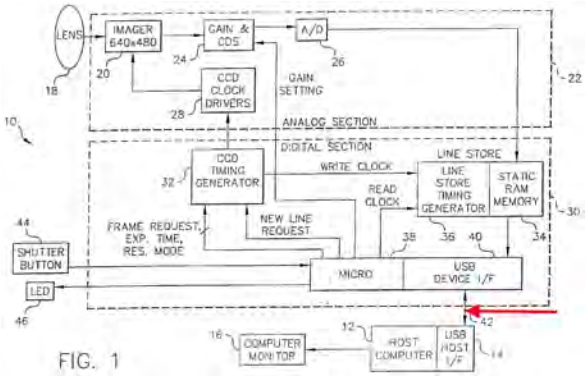
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Dowdy 082 (Figure 4) "FIG. 2 is a block diagram showing in detail the endoscope 2 and the image processing apparatus 3A having the communicating ability which are employed in the present embodiment." (Oshima 212 at 6:34-37.)

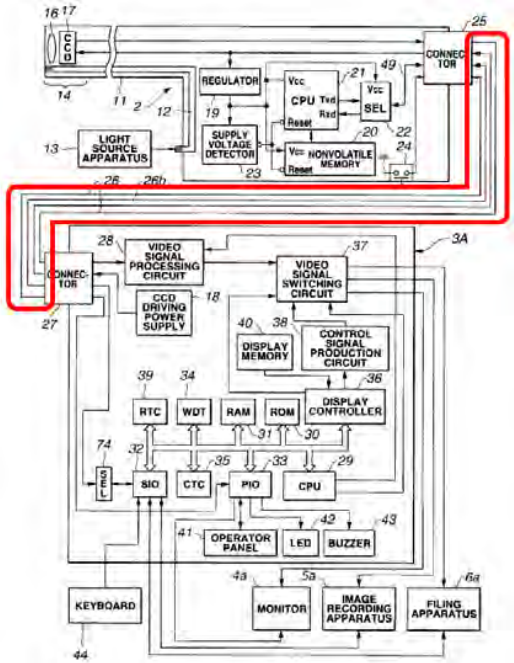
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Oshima 212 (Figure 2) "The image processing apparatus 3A consists broadly of a CCD driving power supply 18, a video signal processing circuit 28, a CPU 29, a ROM 30, a RAM 31, a serial controller (S10) 32, a parallel communication controller (PIO) 33, a watchdog timer (WDT) 34, a counter timer

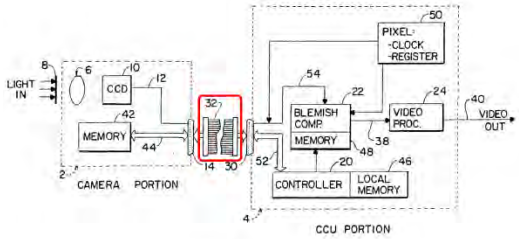
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		(CTC) 35, a display controller 36, a display memory 40, a video signal switching circuit 37, a control signal production circuit 38, a real-time clock (RTC) 39, an operator panel 41, an LED 42, a buzzer 43, and a light adjustment control unit. The CCD driving power supply 18 applies a voltage to the CCD 17 in the endoscope 2. The video signal processing circuit 28 processes a video signal resulting from photoelectric conversion performed by the CCD 17. The CPU 29 carries out a plurality of arithmetic operations." (Oshima 212 at 7:15-27.) "Figure 1 illustrates a prior art video system comprising a camera 2 and a CCU 4. . . . The CCU 4 comprises a controller 20 with local non-volatile digital memory 46, a blemish compensator 22 with associated volatile digital memory 48, a video signal processor 24, a pixel clock/pixel address register 50, a push-button interface and mode selector 28 for directing operation of controller 20." (Zu 391 at 3.)  FIG. 2 Zu 391 (Figure 2)

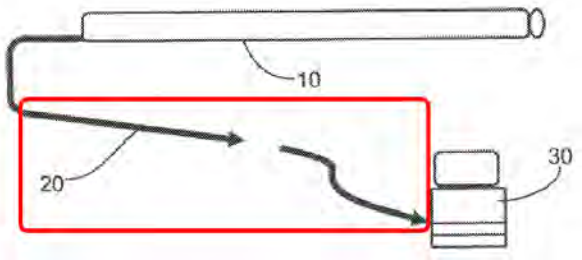
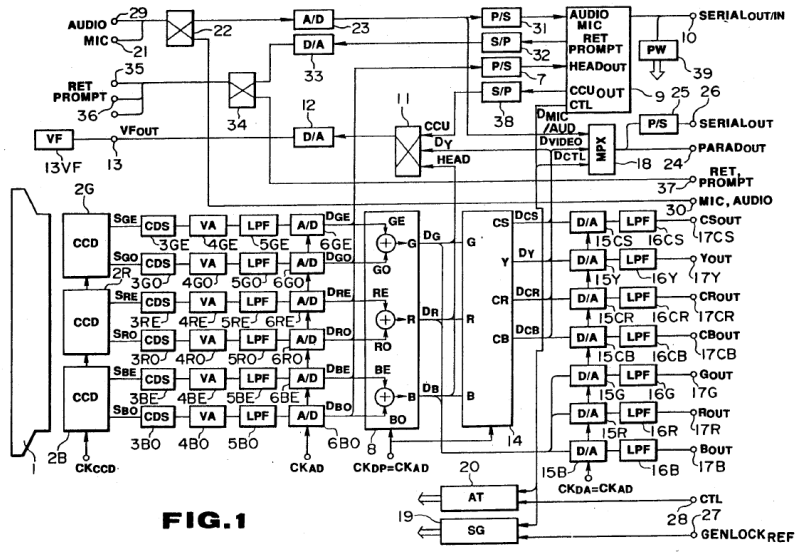
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		"Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope." (Adler 940 at 9:24-33.) "The software included with processing device 30 processes the output of the miniature endoscopic front-end 10. The software may typically control transfer of the images to the monitor of the PC 30 and their display thereon including steps of 3D modeling based on stereoscopic information as will be described below, and may control internal features of the endoscopic front end 10 including light intensity, and automatic gain control (AGC), again as will be described below." (Adler 940 at 9:39-47.) 

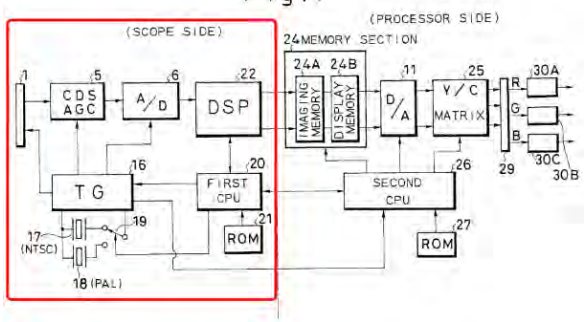
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		Adler 940 (Figure 1)
a cable, connected to said camera control unit, for transmitting the stream of digital video data to said camera control unit; and	"The camera control unit CCU, constituting part of the video camera according to the present invention, is provided with a serial input/output port 40, as shown in FIG. 3, which is connected to the serial input/output port 10 of the camera head unit by an optical fiber cable, not shown, constituting transmission means." (Asaida 782 at 8:5-10 (emphasis added).)	"The camera 10 includes an optical section 18 for imaging light from a subject upon an electronic image sensor 20. A preferred image sensor is a Kodak KAI-0320CM interline transfer, progressive-scan charge-coupled-device (CCD) image sensor with a usable active image area having 640 columns and 480 rows of color photoelements arranged in the well-known Bayer color filter array pattern (see U.S. Pat. No. 3,971,065 for a description of the Bayer pattern)." (Endsley 613 at 3:24-31.) "An analog section 22 in the camera 10 includes the sensor 20, a CDS/gain block 24 for performing correlated double sampling (CDS) and setting the analog gain, an analog-to-digital (A/D) converter 26 for converting the analog output signal from the CCD sensor 20 to, e.g., an 8-bit digital signal, and CCD clock drivers 28 for clocking the sensor 20." (Endsley 613 at 3:31-37.)  FIG. 1

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		Endsley 613 (Figure 1) "The system includes a camera 10 connected to a host computer 12 via a USB (universal serial bus) cable 42 connected to a USB digital host interface 14, which also provides power to the camera 10. . . . The camera 10 can acquire both still and motion images. The camera data is processed by the host computer 12 to create final images that can be displayed on a computer monitor 16, e.g., transmitted along with audio as part of a 'computer videoconference', etc." (Endsley 471 at 2:50-63.) "The USB cable 42 includes four wires, one pair for sending data to and from the host computer 12, and a second pair to supply power to the camera 10 from the host." (Endsley 471 at 3:46-48.)  FIG. 1

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		Endsley 471 (Figure 1) "The connector 25 of the endoscope 2 is linked to a connector 27 of the image processing apparatus 3A by a cable 26." (Oshima 212 at 7:11-13.)  Oshima 212 (Figure 2) "The CCU 4 also comprises an input connector 30 whereby the CCU may be coupled to camera output connector 14 via a suitable cable 32." (Zu 391 at 3.)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 FIG. 2 Zu 391 (Figure 2) "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope. The skilled person will appreciate that the wire connection 20 may be an optical connection or may instead use RF or a like means of wireless communication. The miniature endoscopic front-end 10 may be designed for connection to any standard PC input (the USB input for example)." (Adler 940 at 9:24-38.)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Adler 940 (Figure 1)
a camera head, connected to said cable, for providing the stream of digital video data, said camera head including;	"FIG. 1 is a block diagram showing an embodiment of a camera head unit of a video camera according to the present invention." (Asaida 782 at 3:44-46.)  FIG.1	"In FIG. 1 and FIG. 2, the circuit configuration of an electronic endoscope according to the embodiment is shown. In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having a number of scanning lines or the like suitable for the scanning line of the NTSC system, and to this CCD 1, a timing generator 16 is connected, and to this timing generator 16, an NTSC crystal oscillator 17, a PAL crystal oscillator 18, and a switching device 19 are provided. Furthermore, a first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU 20, either of the oscillators 17, 18 is selected." (Okada 852 at 4:4-15.)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
	Asaida 782 (Figure 1) "The encoder/decoder 9 encodes the serial data, that is, the camera output data $HEAD_{OUT}$, supplied from the P/S converter 7, and outputs the encoded data at a serial input/output port 10 over an optical fiber cable, not shown." (Asaida 782 at 5:45-49.) "Thus, with the present video camera unit, the two-line-concurrent three-color imaging output signals S_{RO}, S_{RE}, S_{GO}, S_{GE}, S_{BO} and S_{BE}, obtained by the solid-state image sensors 2R, 2G, and 2B, are changed by the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE into two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}. The two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, are converted by the P/S converter 7 into serial data as the camera output data $HEAD_{OUT}$, which are serially outputted at the serial input/output port 10 by means of the encoder/decoder 9." (Asaida 782 at 5:50-61.)	Fig. 1  Okada 852 (Figure 1) "The camera 10 includes an optical section 18 for imaging light from a subject upon an electronic image sensor 20. A preferred image sensor is a Kodak KAI-0320CM interline transfer, progressive-scan charge-coupled-device (CCD) image sensor with a usable active image area having 640 columns and 480 rows of color photoelements arranged in the well-known Bayer color filter array pattern (see U.S. Pat. No. 3,971,065 for a description of the Bayer pattern)." (Endsley 613 at 3:24-31.) "An analog section 22 in the camera 10 includes the sensor 20, a CDS/gain block 24 for performing correlated double sampling (CDS) and setting the analog gain, an analog-to-digital (A/D) converter 26 for converting the analog output signal from the CCD sensor 20 to, e.g., an 8-bit digital signal, and CCD clock drivers 28 for clocking the sensor 20." (Endsley 613 at 3:31-37.)

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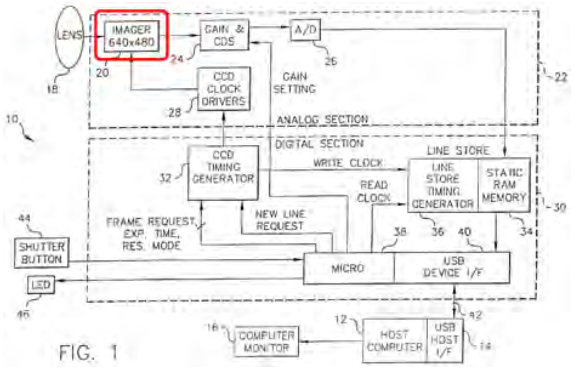
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 FIG. 1 Endsley 613 (Figure 1) "The system includes a camera 10 connected to a host computer 12 via a USB (universal serial bus) cable 42 connected to a USB digital host interface 14, which also provides power to the camera 10. . . . The camera 10 can acquire both still and motion images. The camera data is processed by the host computer 12 to create final images that can be displayed on a computer monitor 16, e.g., transmitted along with audio as part of a 'computer videoconference', etc." (Endsley 471 at 2:50-63.)

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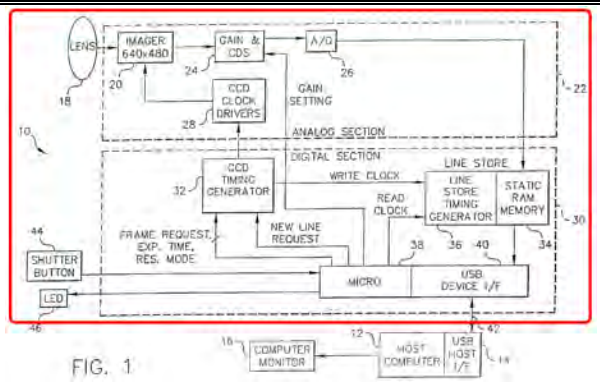
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 FIG. 1 Endsley 471 (Figure 1) "Referring to FIG. 1, a video endoscopy or borescope system 10 includes a camera head 12 and a camera processor 14. Camera head 12 includes an endoscope 16 for insertion into a region such as a body cavity, and an imaging device, such as a CCD 18, that produces electrical signals representative of an optical image at the distal end of endoscope 16. Camera processor 14 processes the electrical signals produced by camera head 12 to generate a video image that is displayed on a video monitor 20." (Dowdy 082 at 3:24-32.) "By varying parameters such as the type of endoscope, the endoscope mount, and the CCD optical format size, camera head 12 can be configured in numerous ways, all of which can produce different electrical signals to represent the same optical image. As illustrated in FIG. 1, camera head 12A

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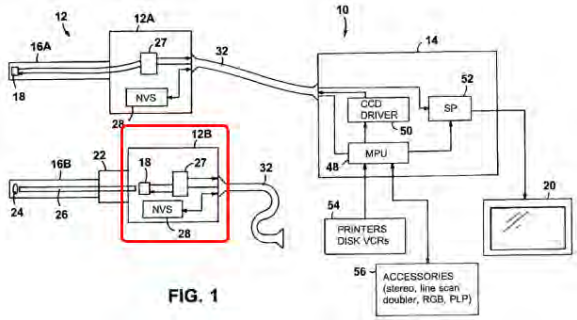
Claims	**Asaida 782**	**in combination with one or more of the following references**
		includes an electronic endoscope 16A, while camera head 12B includes an optical endoscope 16B. Electronic endoscope 16A is integrally connected to camera head 12A and has a CCD 18 positioned behind focussing optics (not shown) at its distal end. By contrast, optical endoscope 16B has a mount 22 for attachment to camera head 12B, and includes an optical lens 24 positioned at its distal tip and an optical fiber 26 or relay lens assembly that transmits an image from optical lens 24 to a CCD 18 positioned, with support circuitry 27, within camera head 16B." (Dowdy 082 at 3:33-47 (emphasis added).)  FIG. 1 Dowdy 082 (Figure 1) "Referring to FIG. 4, in a more detailed view, camera head 12 includes CCD 18 (located, as discussed, either in the head or at the tip of the endoscope), NVS 28 and a set of button switches 92 for system control, and camera processor 14 includes a camera controller 94 and a signal processor 96. Cable 32, which connects camera head 12 to camera

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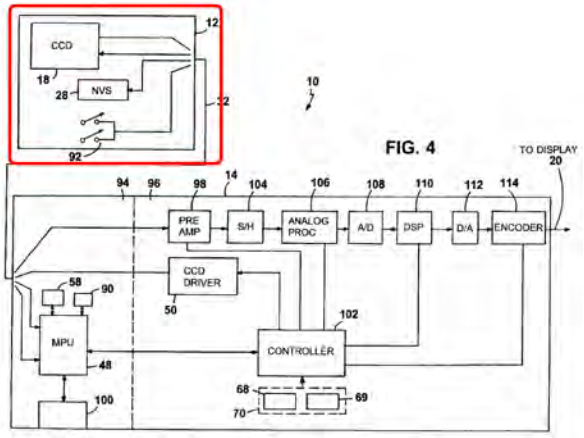
Claims	**Asaida 782**	**in combination with one or more of the following references**
		processor 14, carries drive signals from CCD driver 50 in signal processor 96, electrical signals from CCD 18 to a preamplifier 98 in signal processor 96, data between NVS 28 and MPU 48 in camera controller 94, and signals from button switches 92 to MPU 48." (Dowdy 082 at 6:48-58 (emphasis added).)  Dowdy 082 (Figure 4) "An endoscope system 1 in accordance with the first embodiment of the present invention shown in FIG. 1 consists broadly of an endoscope 2, and connected apparatuses (or peripheral equipment) to be selectively connected to the endoscope. The connected apparatuses include an image processing apparatus 3A, an image processing apparatus 3B, a cleaning apparatus 3C, a filing apparatus 3D, a monitor 4 a, an image recording apparatus 5

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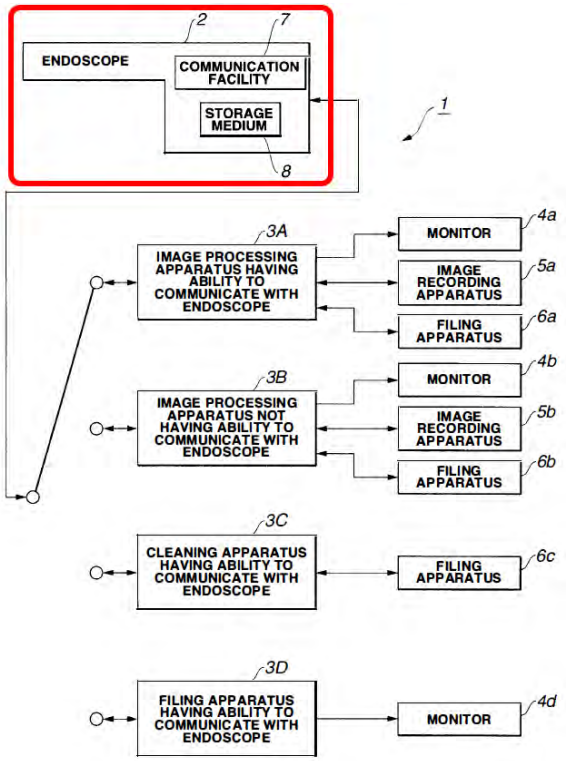
Claims	**Asaida 782**	**in combination with one or more of the following references**
		a, a filing apparatus 6 a, a monitor 4 b, an image recording apparatus 5 b, a filing apparatus 6 b, a filing apparatus 6 c, and a monitor 4 d. The image processing apparatus 3A has the ability to communicate with the endoscope 2. . . ." (Oshima 212 at 5:15-26.)  Oshima 212 (Figure 1)

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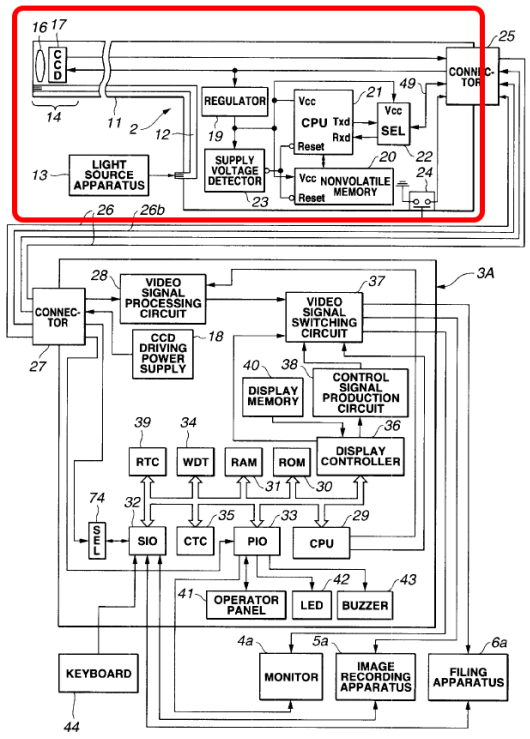
Claims	**Asaida 782**	**in combination with one or more of the following references**
		"FIG. 2 is a block diagram showing in detail the endoscope 2 and the image processing apparatus 3A having the communicating ability which are employed in the present embodiment." (Oshima 212 at 6:34-37.)  Oshima 212 (Figure 2) "The connector 25 of the endoscope 2 is linked to a connector 27 of the image processing apparatus 3A by a

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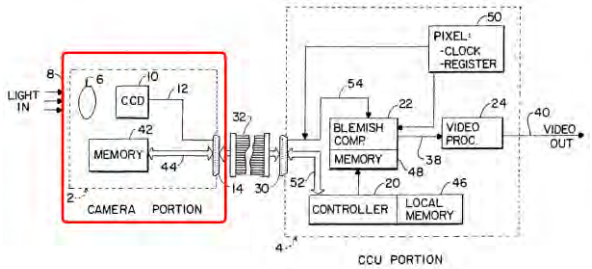
Claims	**Asaida 782**	**in combination with one or more of the following references**
		cable 26." (Oshima 212 at 7:11-13.) "Figure 1 illustrates a prior art video system comprising a camera 2 and a CCU 4. The camera comprises an optical system 6 and a CCD array 10. The latter produces a video signal output when it is illuminated with light via optical system 6. This video signal output is fed by an internal transmission bus 12 to an output connector 14 which forms part of the camera." (Zu 391 at 3.)  FIG. 2 Zu 391 (Figure 2) "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having

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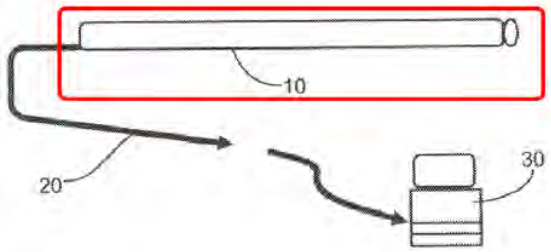
Claims	**Asaida 782**	**in combination with one or more of the following references**
		appropriate software for carrying out image processing of the output of the endoscope. The skilled person will appreciate that the wire connection 20 may be an optical connection or may instead use RF or a like means of wireless communication. The miniature endoscopic front-end 10 may be designed for connection to any standard PC input (the USB input for example)." (Adler 940 at 9:24-38.)  Adler 940 (Figure 1)
an imager, for generating an analog stream of video data;	"In the camera head unit, shown in FIG. 1, the present invention includes a three CCD solid state color imaging device in which the imaging light from an object in a field of view is separated by an imaging pickup device 1 into three primary color components and in which three primary color object images are produced by three solid state imaging sensors 2R, 2G and 2B." (Asaida 782 at 4:9-15.)	"In FIG. 1 and FIG. 2, the circuit configuration of an electronic endoscope according to the embodiment is shown. In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having a number of scanning lines or the like suitable for the scanning line of the NTSC system, and to this CCD 1, a timing generator 16 is connected, and to this timing generator 16, an NTSC crystal oscillator 17, a PAL crystal oscillator 18, and a switching device 19 are provided. Furthermore, a first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU 20,

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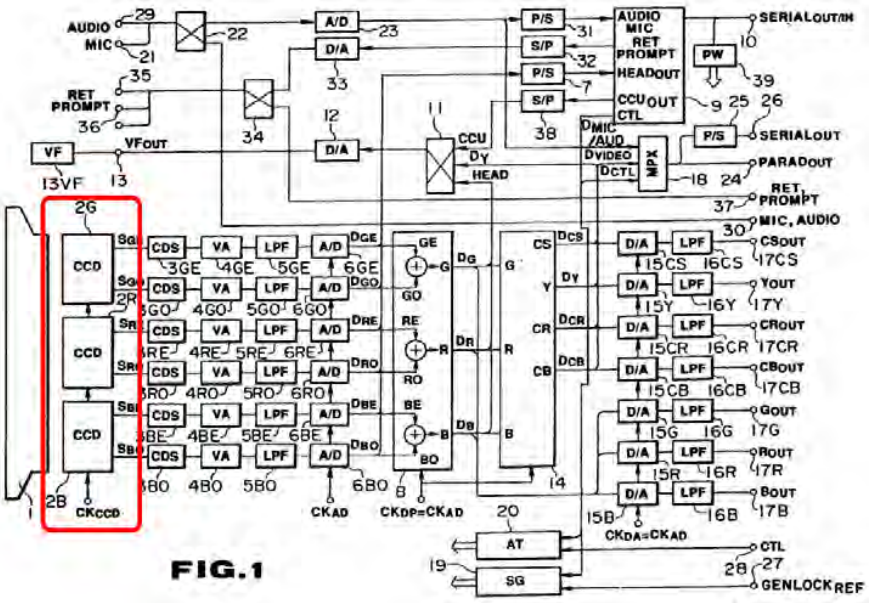
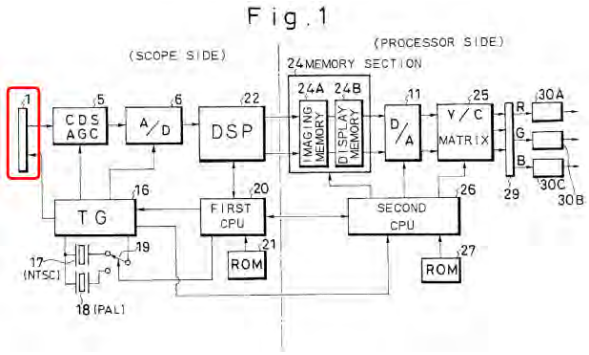
Claims	**Asaida 782**	**in combination with one or more of the following references**
	 FIG.1 Asaida 782 (Figure 1)	either of the oscillators 17, 18 is selected." (Okada 852 at 4:4-15.)  Okada 852 (Figure 1) "The camera 10 includes an optical section 18 for imaging light from a subject upon an electronic image sensor 20. A preferred image sensor is a Kodak KAI-0320CM interline transfer, progressive-scan charge-coupled-device (CCD) image sensor with a usable active image area having 640 columns and 480 rows of color photoelements arranged in the well-known Bayer color filter array pattern (see U.S. Pat. No. 3,971,065 for a description of the Bayer pattern)." (Endsley 613 at 3:24-31.) "An analog section 22 in the camera 10 includes the sensor 20, a CDS/gain block 24 for performing correlated double sampling (CDS) and setting the analog gain, an analog-to-digital (A/D) converter 26 for converting the analog output

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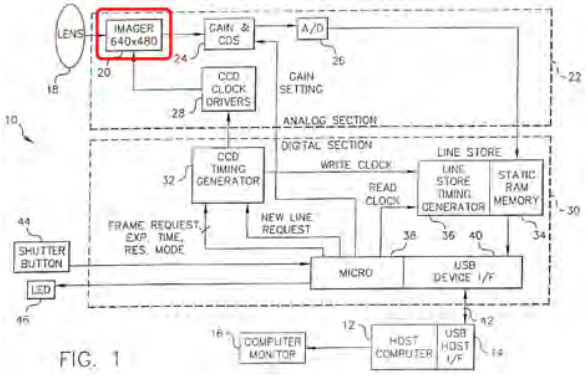
Claims	**Asaida 782**	**in combination with one or more of the following references**
		signal from the CCD sensor 20 to, e.g., an 8-bit digital signal, and CCD clock drivers 28 for clocking the sensor 20." (Endsley 613 at 3:31-37.)  Endsley 613 (Figure 1) "The camera 10 includes an optical section 18 from imaging light from a subject upon an electronic image sensor 20. A preferred image sensor is a Kodak KAI-0320CM interline transfer, progressive-scan charge-coupled-device (CCD) image sensor with a usable active image area having 640 columns and 480 rows of color photoelements arranged in the well-known Bayer color filter array patters shown in FIG. 2 (see U.S. Pat. No. 3,971,065 for further description of the Bayer pattern). As shown in FIG. 2, the sensor 20 includes light shielded vertical registers 50 and a horizontal readout register 52. Details of a single photoelement 54 are shown in FIG. 3. Each photoelement 54 includes a light-sensitive photodiode 56 supported on a substrate 58 adjacent the light-

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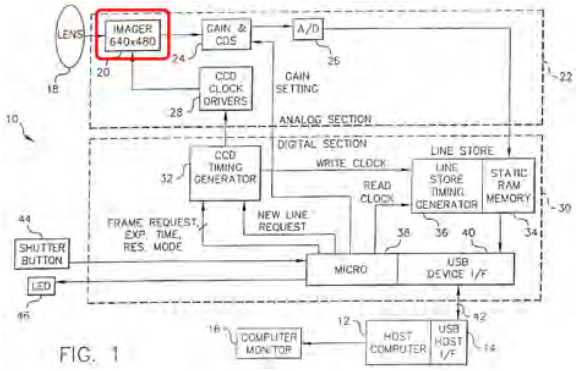
Claims	**Asaida 782**	**in combination with one or more of the following references**
		shielded vertical register 50." (Endsley 471 at 2:66-3:12.) "An analog section 22 in the camera 10 includes the sensor 20, a CDS/gain block 24 for performing correlated double sampling (CDS) and setting the analog gain, an analog-to-digital (A/D) converter 26 for converting the analog output signal from the CCD sensor 20 to, e.g., an 8-bit digital signal, and CCD clock drivers 28 for clocking the sensor 20." (Endsley 471 at 3:13-18.)  FIG. 1 Endsley 471 (Figure 1) "Referring to FIG. 1, a video endoscopy or borescope system 10 includes a camera head 12 and a camera processor 14. Camera head 12 includes an endoscope 16 for insertion into a region such as a body cavity, and an imaging device, such as a CCD 18, that produces electrical signals representative of an optical image at the distal end of endoscope 16. Camera processor 14 processes the electrical signals

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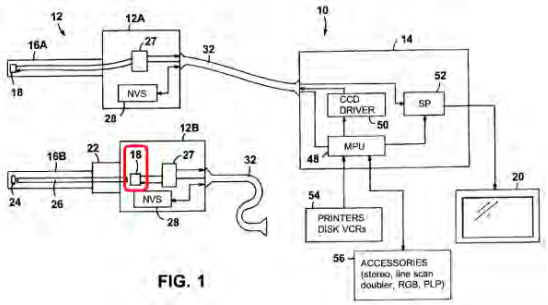
Claims	**Asaida 782**	**in combination with one or more of the following references**
		produced by camera head 12 to generate a video image that is displayed on a video monitor 20." (Dowdy 082 at 3:24-32.) "By varying parameters such as the type of endoscope, the endoscope mount, and the CCD optical format size, camera head 12 can be configured in numerous ways, all of which can produce different electrical signals to represent the same optical image. As illustrated in FIG. 1, camera head 12A includes an electronic endoscope 16A, while camera head 12B includes an optical endoscope 16B. Electronic endoscope 16A is integrally connected to camera head 12A and has a CCD 18 positioned behind focussing optics (not shown) at its distal end. By contrast, optical endoscope 16B has a mount 22 for attachment to camera head 12B, and includes an optical lens 24 positioned at its distal tip and an optical fiber 26 or relay lens assembly that transmits an image from optical lens 24 to a CCD 18 positioned, with support circuitry 27, within camera head 16B." (Dowdy 082 at 3:33-47 (emphasis added).)  FIG. 1

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		Dowdy 082 (Figure 1) "The output of preamplifier 98 is connected to the input of a sample and hold circuit 104 that passes only portions of the output. The output of sample and hold circuit 104 is supplied to an analog processing circuit 106 that is also controlled by signal processing controller 102. In controlling analog processing circuit 106, signal processing controller 102 uses values from lookup table 68 that have been loaded into memory 70. As discussed above, if these values have been modified or replaced by MPU 48 based on information from NVS 28 of camera head 12, then analog processing circuit 106 will be affected by the new values." (Dowdy 082 at 7:27-37.) "An analog to digital converter 108 converts the output of analog processing circuit 106 into a digital signal, and supplies the digital signal to a digital signal processor (DSP) 110 that is controlled by signal processing controller 102. Once again, signal processing controller 102 controls digital signal processor using values from memory 70 that can be modified or replaced by MPU 48 in response to information from NVS 28 of camera head 12." (Dowdy 082 at 7:38-45.) Because digital-to-analog conversion takes place in the CCU, the imager 18 must generate an analog stream of video data. "The illuminated object is imaged by a solid-state imaging device located on an image plane, for example, a charge-

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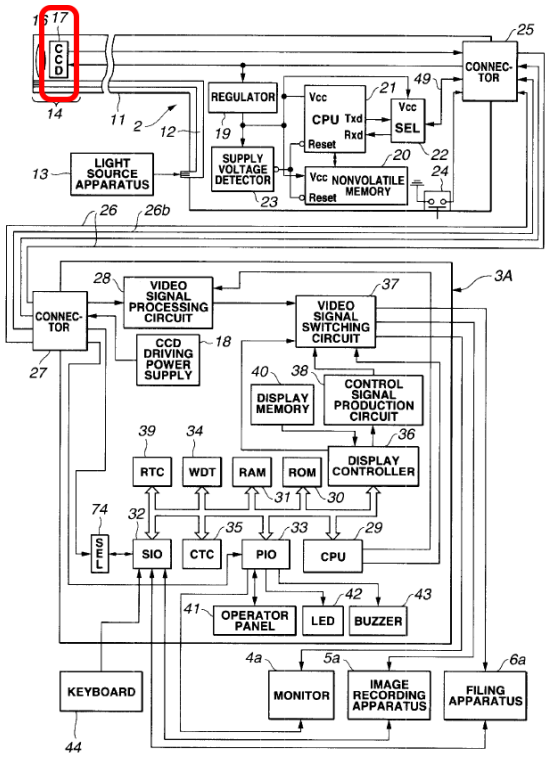
Claims	**Asaida 782**	**in combination with one or more of the following references**
		coupled device (CCD) 17 through an objective 16 locked in an observation window formed in the distal part 14. The CCD 17 photoelectrically converts the optical image." (Oshima 212 at 6:49-53.)



Oshima 212 (Figure 2)

"Figure 1 illustrates a prior art video system comprising a

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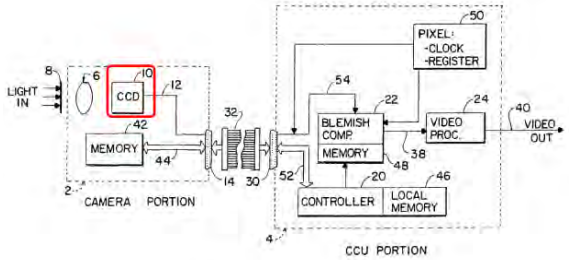
Claims	**Asaida 782**	**in combination with one or more of the following references**
		camera 2 and a CCU 4. The camera comprises an optical system 6 and a CCD array 10. The latter produces a video signal output when it is illuminated with light via optical system 6. This video signal output is fed by an internal transmission bus 12 to an output connector 14 which forms part of the camera." (Zu 391 at 3 (emphasis added).)  FIG. 2 Zu 391 (Figure 2) "Reference is now made to FIG. 2, which is an internal block diagram of an endoscope according to a preferred embodiment of the present invention. A miniature endoscope 40 is connected by a wire 42 to an adapter 44. The endoscope 40 comprises an image sensor 46 which may typically comprise a CMOS or CCD or like sensing technology, an optical assembly 48, a light or illumination source 50, communication interface 52 and controller 54. The wired unit of FIG. 2 preferably includes a voltage regulator 56." (Adler 940 at 9:48-57.)

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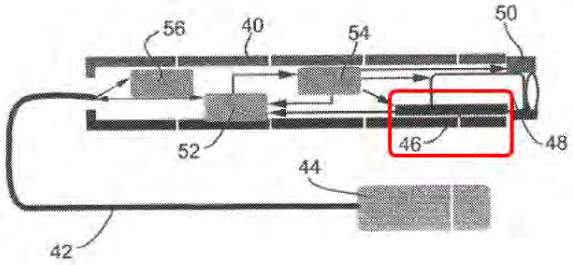
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Adler 940 (Figure 2) "The present invention relates generally to the field of interface circuits, and more particularly, to interface circuitry for providing selectable single-ended and differential signal output from a CMOS image sensor to an external digital signal processor." (Chung 290 at 1:11-15.) "One of the advantages of CMOS image sensors (CMOS imagers) over CCD imagers is that the CMOS imager chip can include digital signal processing circuitry. In practice, the signal processing is more often performed on a companion chip, in order to provide greater application flexibility. However, CMOS imagers often have integrated analog to digital converters to convert the analog signal to a digital bit stream that can be processed by the companion chip. The digitized information then must be transferred to companion chip or other external devices for picture storage, processing, or transmission." (Chung 290 at 1:17-27.) "FIG. 4 illustrates CMOS video imaging sensing circuitry

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		according to the preferred embodiment disclosed in co-pending U.S. application Ser. No 09/062,343. This circuitry includes a CMOS image sensor chip 50 and an image processor chip 52. The CMOS image sensor chip 50 typically includes a number of light responsive CMOS pixel sensors which develop analog signals representative of an image. These analog signals are then A to D converted by the ADC circuit to form digital signals Din0, Din1 . . . Dinn. The image processor chip 52 includes a data processor 53 which performs various manipulations of the image data such as compression and color processing. The processor 53 may be software driven or a hardware embodiment." (Chung 290 at 2:14-26.)

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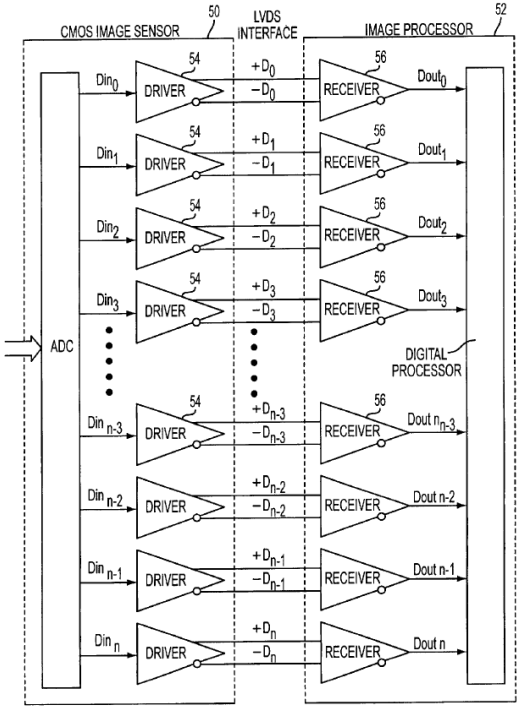
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Chung 290 (Figure 4)
a converter, for converting the analog stream of video data into the	"The two-line-concurrent three-color imaging output signals S_{RO}, S_{RE}, S_{GO}, S_{GE}, S_{BO} and S_{BE}, processed for level adjustment by the level adjustment circuits 4RO, 4RE, 4GO, 4GE, 4BO and 4BE, are transmitted by means of low-pass filters 5RO, 5RE, 5GO, 5GE, 5BO and 5BE, respectively, to A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, functioning as analog/ digital converting means, respectively." (Asaida 782 at 5:14-22.)	"[T]o the CCD 1, an AGC (automatic gain control) circuit including a CDS (correlative double sampling) circuit is connected similarly to that in the prior art, and to this AGC circuit 5, a DSP (digital signal processor) circuit 22 is connected through an A/D converter 6." (Okada 852 at 4:29-33.)

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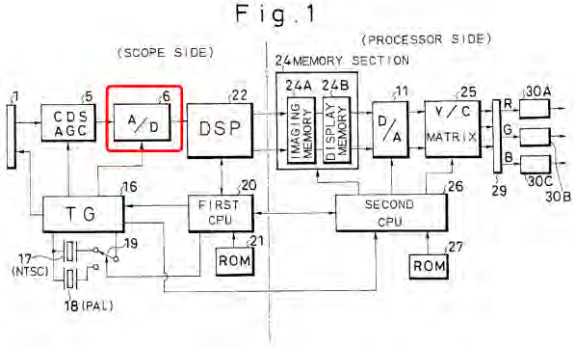
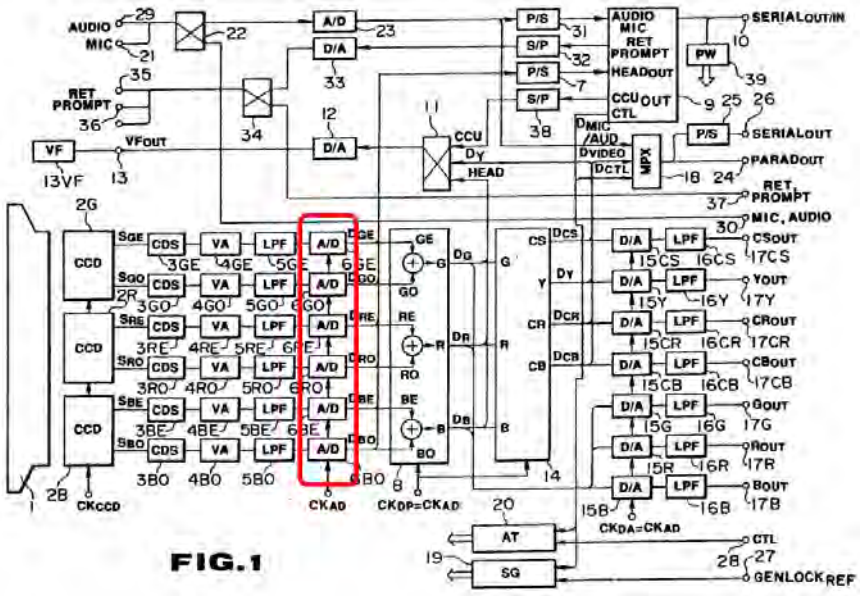
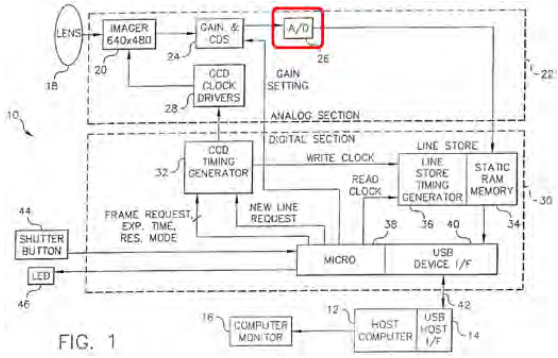
Claims	**Asaida 782**	**in combination with one or more of the following references**
stream of digital video data;	"A driving clock CK_{AD} having a frequency four times the frequency of the color subcarrier frequency f_{SC}, or $4f_{SC}$, is supplied to the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, by means of a timing generator, not shown. The A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE digitize the two-line-concurrent three-color imaging output signals S_{RO}, S_{RE}, S_{GO}, S_{GE}, S_{BO} and S_{BE} with the $4f_{sc}$ driving clock CK_{AD} to produce two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, respectively. The two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, produced by the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, are supplied to a parallel/serial converter (P/S converter) 7 and to a signal processing section 8." (Asaida 782 at 5:23-37.)	Fig. 1  Okada 852 (Figure 1) "A digital section 30 includes a CCD timing generator 32, a static RAM memory 34, a line store timing generator 36, a microprocessor 38, and a USB device interface 40." (Endsley 613 at 3:38-40.) "The microprocessor 38, which may be the Intel 82930 microprocessor, reads data from the line store 34, and transfers the data t the computer 12 via the USB interface 40 (which may be incorporated as part of the microprocessor 38)." (Endsley 613 at 3:58-62.) "An analog section 22 in the camera 10 includes the sensor 20, a CDS/gain block 24 for performing correlated double sampling (CDS) and setting the analog gain, an analog-to-digital (A/D) converter 26 for converting the analog output signal from the CCD sensor 20 to, e.g., an 8-bit digital signal, and CCD clock drivers 28 for clocking the sensor 20."

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
	 FIG.1 Asaida 782 (Figure 1)	(Endsley 471 at 3:13-18.)  FIG. 1 Endsley 471 (Figure 1) "Reference is now made to FIG. 4, which is an schematic block diagram of the miniature endoscope according to a preferred embodiment of the present invention. Parts that are identical to those shown above are given the same reference numerals and are not referred to again except as necessary for an understanding of the present embodiment. Optical assembly 48 receives light, indicated by arrows 60, from an object being viewed. The light is processed by optical assembly 48, as will be explained below, to reach image sensor 46 were it is converted from photons into electrical signals. The electrical signals are digitized and passed to a transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Adler 940 at 10:7-19 (emphasis added).)

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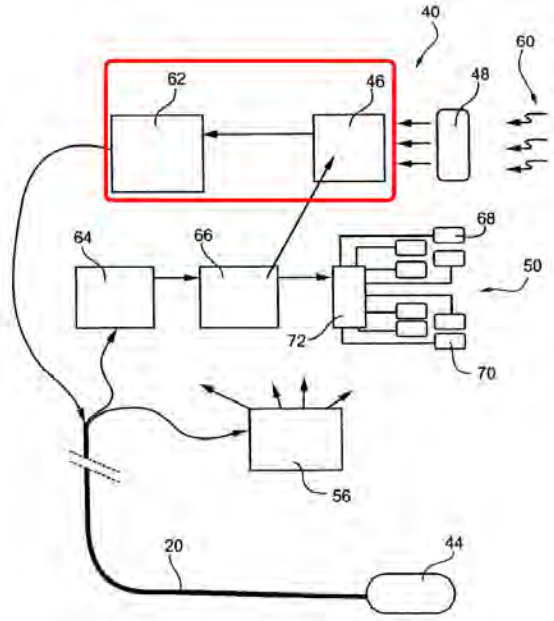
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Adler 940 (Figure 4) Because "the electrical signals are digitized and passed to a transmitting device 62" in the camera head, the camera head must contain a converter for converting an analog stream of video data into a stream of digital video data. "One of the advantages of CMOS image sensors (CMOS imagers) over CCD imagers is that the CMOS imager chip can include digital signal processing circuitry. In practice, the signal processing is more often performed on a companion chip, in order to provide greater application

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		flexibility. However, CMOS imagers often have integrated analog to digital converters to convert the analog signal to a digital bit stream that can be processed by the companion chip. The digitized information then must be transferred to companion chip or other external devices for picture storage, processing, or transmission." (Chung 290 at 1:17-27 (emphasis added).) "FIG. 4 illustrates CMOS video imaging sensing circuitry according to the preferred embodiment disclosed in co-pending U.S. application Ser. No 09/062,343. This circuitry includes a CMOS image sensor chip 50 and an image processor chip 52. The CMOS image sensor chip 50 typically includes a number of light responsive CMOS pixel sensors which develop analog signals representative of an image. These analog signals are then A to D converted by the ADC circuit to form digital signals Din0, Din1 . . . Dinn. The image processor chip 52 includes a data processor 53 which performs various manipulations of the image data such as compression and color processing. The processor 53 may be software driven or a hardware embodiment." (Chung 290 at 2:14-26.)

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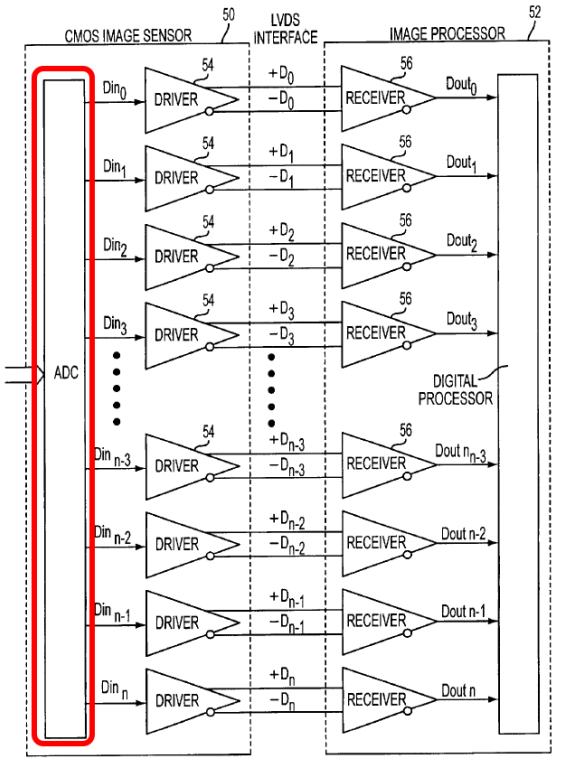
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Chung 290 (Figure 4)
a serializer, for serializing the stream of digital video data	"A driving clock CK_{AD} having a frequency four times the frequency of the color subcarrier frequency f_{SC}, or $4f_{SC}$, is supplied to the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, by means of a timing generator, not shown. The A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE digitize the two-line-concurrent three-color imaging output signals S_{RO}, S_{RE}, S_{GO}, S_{GE}, S_{BO} and S_{BE} with the $4f_{sc}$	"A digital section 30 includes a CCD timing generator 32, a static RAM memory 34, a line store timing generator 36, a microprocessor 38, and a USB device interface 40." (Endsley 613 at 3:38-40.) "The microprocessor 38, which may be the Intel 82930

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Claims	**Asaida 782**	**in combination with one or more of the following references**
	driving clock CK_{AD} to produce two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, respectively. The two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, produced by the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, are supplied to a parallel/serial converter (P/S converter) 7 and to a signal processing section 8." (Asaida 782 at 5:23-37.) "The P/S converter 7 changes the two-line-concurrent digital three color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, supplied from the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO, and 6BE, from parallel data into serial data. The serial data, produced by the P/S converter 7, are supplied as camera output data $HEAD_{OUT}$ to a light-transmitting encoder/decoder 9." (Asaida 782 at 5:38-44.) "The encoder/decoder 9 encodes the serial data, that is, the camera output data $HEAD_{OUT}$, supplied from the P/S converter 7, and outputs the encoded data at a serial input/output port 10 over an optical fiber cable, not shown." (Asaida 782 at 5:45-49.)	microprocessor, reads data from the line store 34, and transfers the data t the computer 12 via the USB interface 40 (which may be incorporated as part of the microprocessor 38)." (Endsley 613 at 3:58-62.) To the extent this element is not expressly disclosed, it is inherent in Endsley 471 by virtue of disclosing and claiming USB as a communications medium. Specifically, section 10.2.2 of the USB Specification Revision 1.0 (Jan. 15, 1996) explains that "[t]he actual transmission of data across the physical USB takes place as a serial bit stream. A Serial Interface Engine (SIE), whether implemented as part of the host or a USB device, handles the serialization and deserialization of USB transmissions. On the host, this SIE is part of the host controller." (USB Spec. Rev. 1.0 at 200.) Thus, in order for USB to be implemented as disclosed and claimed in Endsley 471, there must be "a serializer, for serializing the stream of digital video data for transmission over said cable."

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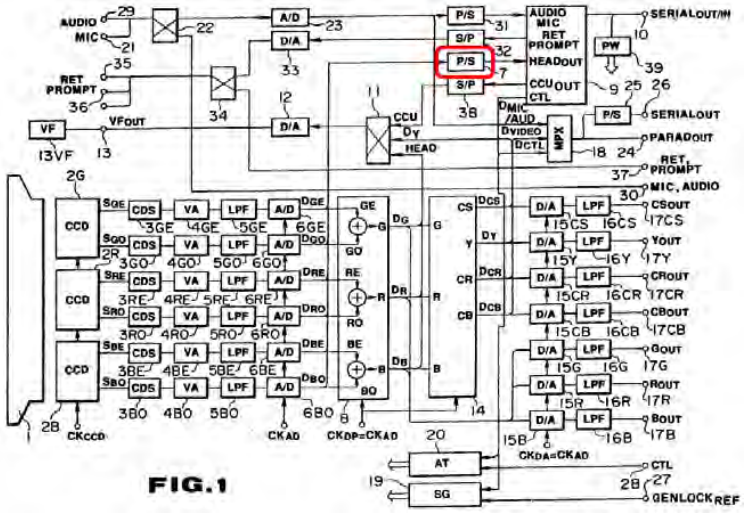
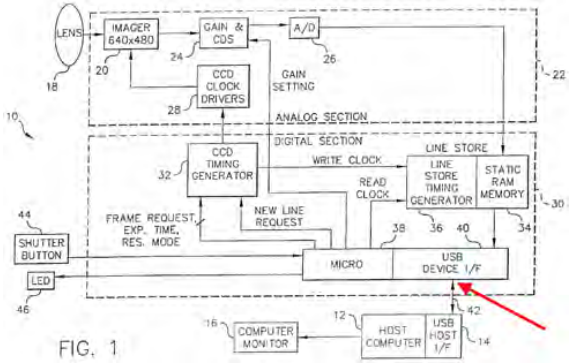
Claims	**Asaida 782**	**in combination with one or more of the following references**
	 FIG.1 Asaida 782 (Figure 1)	 FIG. 1 Endsley 471 (Figure 1) "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope. The skilled person will appreciate that the wire connection 20 may be an optical connection or may instead use RF or a like means of wireless communication. The miniature endoscopic front-end 10 may be designed for connection to any standard PC input (the USB input for example)." (Adler 940 at 9:24-38 (emphasis added).)

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		"Reference is now made to FIG. 4, which is an schematic block diagram of the miniature endoscope according to a preferred embodiment of the present invention. Parts that are identical to those shown above are given the same reference numerals and are not referred to again except as necessary for an understanding of the present embodiment. Optical assembly 48 receives light, indicated by arrows 60, from an object being viewed. The light is processed by optical assembly 48, as will be explained below, to reach image sensor 46 were it is converted from photons into electrical signals. The electrical signals are digitized and passed to a transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Adler 940 at 10:7-19 (emphasis added).) Because both USB and LVDS are contemplated by Adler 940 as a means for transmitting the stream of digital video data over cable 20, both of which are serial communication protocols, the camera head must include a component that a serializes the digital video data.
a processor; and	"The signal processing section 8 adds the two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, supplied from the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, for each of the color signals, in such a manner that switching between upper and lower lines on both sides of a center line is done on a field-by-field basis to form interlaced digital three-color signals D_R, D_G and D_B. The signal processing section 8 also processes the digital three color	"In FIG. 1 and FIG. 2, the circuit configuration of an electronic endoscope according to the embodiment is shown. In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having a number of scanning lines or the like suitable for the scanning line of the NTSC system, and to this CCD 1, a timing generator 16 is connected, and to this timing generator 16, an NTSC crystal

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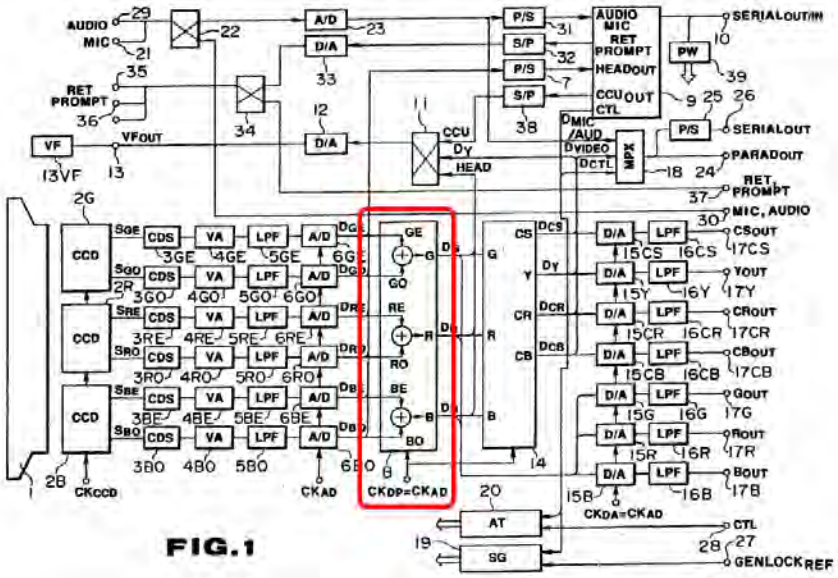
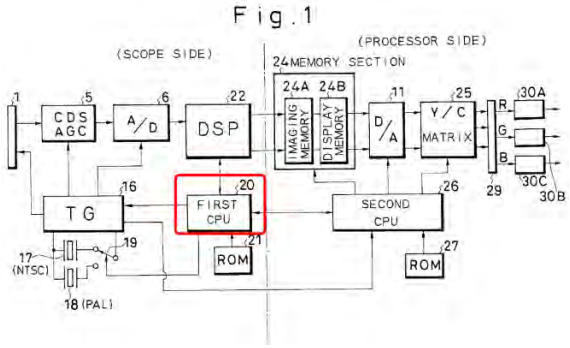
Claims	**Asaida 782**	**in combination with one or more of the following references**
	signals D_R, D_G and D_B using, for example, gamma correction and image enhancement." (Asaida 782 at 5:62-6:4.)  FIG.1 Asaida 782 (Figure 1) Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005) (citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)).	oscillator 17, a PAL crystal oscillator 18, and a switching device 19 are provided. Furthermore, a first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU 20, either of the oscillators 17, 18 is selected." (Okada 852 at 4:4-15.)  Fig. 1 Okada 852 (Figure 1) "A digital section 30 includes a CCD timing generator 32, a static RAM memory 34, a line store timing generator 36, a microprocessor 38, and a USB device interface 40." (Endsley 613 at 3:38-40.) "The microprocessor 38, which may be the Intel 82930 microprocessor, reads data from the line store 34, and transfers the data t the computer 12 via the USB interface 40 (which may be incorporated as part of the microprocessor 38)." (Endsley 613 at 3:58-62.)

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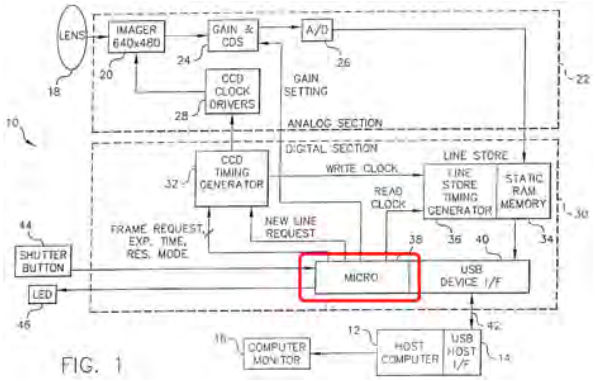
Claims	**Asaida 782**	**in combination with one or more of the following references**
	Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	"A digital section 30 includes a CCD timing generator 32, a static RAM line store memory 34, a line store timing generator 36, a microprocessor 38, and a USB device interface 40." (Endsley 471 at 3:19-22.) "The USB interface 40, which may be incorporated as part of the microprocessor 38, such as the Intel 82930 microprocessor, reads data from the line store 34." (Endsley 471 at 3:43-46.)  Endsley 471 (Figure 1) "As shown in FIG. 1, camera processor 14 includes a microprocessing unit ("MPU") 48, a CCD driver 50, and signal processing ("SP") circuitry 52. In operation, MPU 48 provides control to CCD driver 50 for transmitting driving signals to CCD 18 in camera head 12. In response to the

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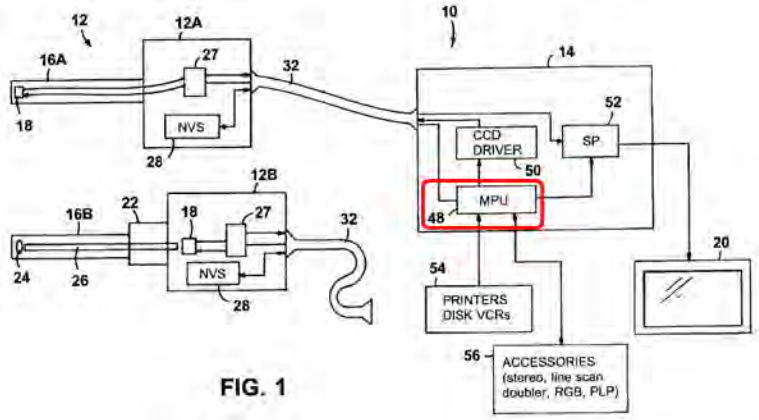
Claims	**Asaida 782**	**in combination with one or more of the following references**
		driving signals, CCD 18 produces electrical signals representing an image of objects within the field of view of CCD 18, and transmits the electrical signals to signal processing circuitry 52. Signal processing circuitry 52 processes the electrical signals from CCD 18 and converts them to video signals for displaying the image on video monitor 20." (Dowdy 082 at 4:60-5:3.)  FIG. 1 Dowdy 082 (Figure 1) "Referring also to FIG. 3, MPU 48 uses the information stored in NVS 28 to control the operation of CCD driver 50 and signal processing circuitry 52. When the user connects cable 32 of camera head 12 to camera processor 14, and, if necessary, powers up video endoscopy system 10, MPU 48 detects the connection and responds by downloading the information from NVS 28 into a memory 58, such as a RAM,

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		of MPU 48 (step 200). MPU 48 reads the stored information out of NVS 28 through a serial data link in cable 32 that includes a CLOCK line 60 controlled by MPU 48 and a DATA line 62 that is shared by NVS 28 and MPU 48." (Dowdy 082 at 5:9-19.) "MPU 48 communicates with signal processing circuitry 52 through a bidirectional serial data link that includes a CLOCK line 80 controlled by MPU 48 and a DATA line 82 that is shared by MPU 48 and signal processing circuitry 52. MPU 48 also controls an ENABLE line 84 that activates external control of signal processing circuitry 52." (Dowdy 082 at 6:1-6.) "After modifying the values of table entries 72-78 received from signal processing circuitry 52, MPU 48 transmits the updated values to signal processing circuitry 52 (step 218). When entries from NVS 28 reflect replacement values for entries in lookup table 68, MPU 48 transmits the replacement values (step 218) without requesting values from signal processing circuitry and modifying those values (steps 208-216)." (Dowdy 082 at 6:18-25.) "After signal processing circuitry 52 receives the updated values from MPU 48 (step 220), signal processing circuitry 52 uses the updated values in processing the electrical signals from CCD 18 for display on video monitor 20 (step 222). That is, signal processing circuitry 52 uses the updated values in locations 69—rather than the nominal values from lookup table 68—in performing the conversion of the

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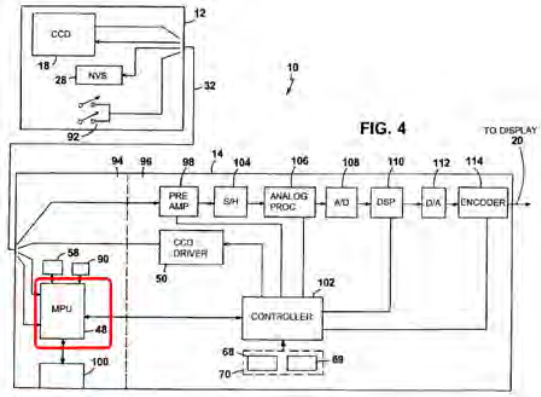
Claims	**Asaida 782**	**in combination with one or more of the following references**
		electrical signals from CCD 18 to video signals." (Dowdy 082 at 6:26-33.) "Referring to FIG. 4, in a more detailed view, camera head 12 includes CCD 18 (located, as discussed, either in the head or at the tip of the endoscope), NVS 28 and a set of button switches 92 for system control, and camera processor 14 includes a camera controller 94 and a signal processor 96. Cable 32, which connects camera head 12 to camera processor 14, carries drive signals from CCD driver 50 in signal processor 96, electrical signals from CCD 18 to a preamplifier 98 in signal processor 96, data between NVS 28 and MPU 48 in camera controller 94, and signals from button switches 92 to MPU 48." (Dowdy 082 at 6:48-58.)  Dowdy 082 (Figure 4) "MPU 48 controls signal processor 96 in response to signals

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		from button switches 92 and signals from controls in a front panel 100 of camera controller 94. The controls in front panel 100 allow the user of video endoscopy system 10 to configure button switches 92 to perform desired functions. Thus, for example, button switches 92 could be configured to cause signal processor 96 to pause the video image displayed at video monitor 20 (FIG. 1). MPU 48 also displays system parameters at front panel 100, interacts with NVS 28 by downloading information about camera head 12 and updating run time information in NVS 28, updates signal processing parameters in light of the information about camera head 12, and communicates with signal processor 96, all as discussed above." (Dowdy at 6:59-7:5.) Although MPU 48 is located in camera processor 14, it is contained within camera controller 94 which is independent of camera processor 96. Because camera controller 94 and camera processor 96 are independent units housed within camera processor 14, camera controller 94 (and as a result, MPU 48) could have been located in camera head 12. Locating camera controller 94 in the camera head 12 would have been a design option attractive to one of ordinary skill in the art looking to minimize communication circuitry between NVS 28 and MPU 48, as both would be housed within camera 12. "A regulator 19, a programmable nonvolatile memory 20, a CPU 21, a selector (SEL) 22, a supply voltage detector 23, a scope switch 24, and a connector 25 are arranged behind the rear end of the insertion unit 11 of the endoscope 2. The

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		regulator 19 converts a CCD driving voltage fed from a CCD driving power supply 18 incorporated in the image processing apparatus 3A into a desired voltage. The programmable nonvolatile memory 20 in which the endoscope-related data is stored is realized with an EEPROM, a flash ROM, an FRAM, or an MRAM." (Oshima 212 at 6:54-63.) "The CPU 21 includes a one-chip microcomputer for performing a plurality of arithmetic operations including communication and writing, or reading. Specifically, the CPU 21 transmits or receives the endoscope-related data to or from the image processing apparatus 3A through a serial interface, and writes or reads the endoscope-related data in or from the nonvolatile memory 20. The CPU 21 includes a ROM, a RAM, a watchdog timer (WDT), a serial controller (S10), a parallel controller (P10), and a counter (CTC). The selector 22 acts as a serial interface means for transmitting or receiving the endoscope-related data over a sole signal line 49. The supply voltage detector 23 detects a fluctuation or drop in supply voltage and outputs a reset signal, thus preventing a malfunction of the CPU 21 or the nonvolatile memory 20." (Oshima 212 at 6:63-7:10.)

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		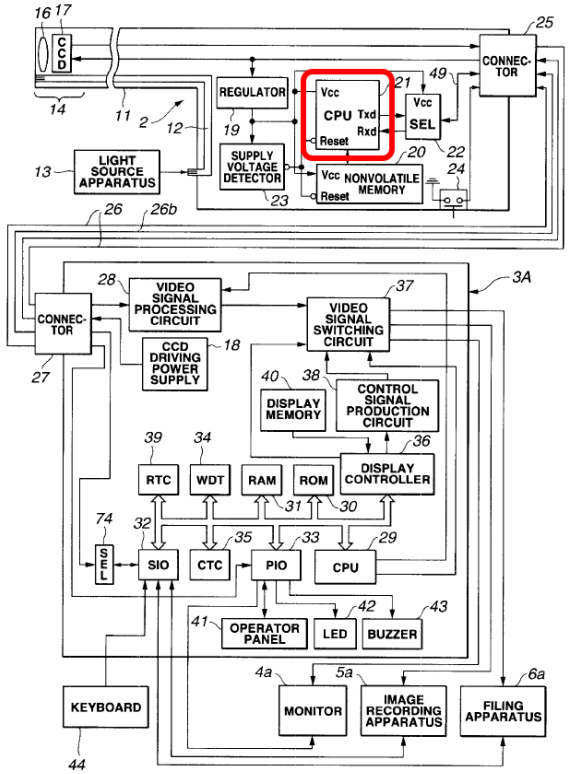 Oshima 212 (Figure 2)
a memory device, accessible by said processor,	Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005)	"In FIG. 1 and FIG. 2, the circuit configuration of an electronic endoscope according to the embodiment is shown. In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having a number of scanning lines or the like suitable for the scanning line of the

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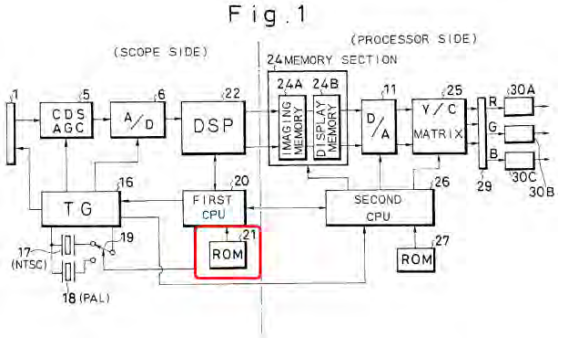
Claims	**Asaida 782**	**in combination with one or more of the following references**
containing camera head information.	(citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)). Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	NTSC system, and to this CCD 1, a timing generator 16 is connected, and to this timing generator 16, an NTSC crystal oscillator 17, a PAL crystal oscillator 18, and a switching device 19 are provided. Furthermore, a first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU 20, either of the oscillators 17, 18 is selected." (Okada 852 at 4:4-15.)  Okada 852 (Figure 1) "The NTSC crystal oscillator 17 generates a signal with a frequency of about 14.32 MHz (N·fh1), and the PAL oscillator 18 on the other side may be an oscillator which generates a signal with the above mentioned frequency of about 17.73 MHz, but in this example, an oscillator which generates a signal with a frequency of N·fh2 [N times the frequency of the horizontal synchronization signal of 15.625 kHz (=fh2)] near the NTSC oscillation frequency is used.

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		Consequently, the change of the circuit member relating to the drive operation, the setting of a constant, or the like become easy. Moreover, to the first CPU 20, a ROM 21 storing setting data for the control meeting the NTSC system or the PAL system is connected." (Okada 852 at 4:16-28 (emphasis added).) "A first example is configured like the above, and in the example, each television system can be selected by selective switches arranged at the processor or the like, and the state of selection of the switches can be grasped by the second CPU 26. Then, this second CPU 26 reads out the setting data of the selected system from the ROM 27 to set the processing contents of each circuit by this setting data. At the same time, the information of the selected system is also transmitted to the first CPU 20 on the scope side from this second CPU 26, and on this scope side, the selected setting data is read out from the ROM 21 by the first CPU 20 to set the processing contents of each circuit, and further, either of the above oscillators 17, 18 is selected and set." (Okada 852 at 4:58-5:3 (emphasis added).) "The camera 10 is connected to a host computer 12 via a USB (universal serial bus) digital host interface 14, which also provides power to the camera 10. . . . The camera 10 can acquire both still and motion images. The camera data is processed by the host computer 12 to create final images that can be displayed on a computer monitor 16, e.g., transmitted along with audio as part of a "computer videoconference", etc." (Endsley 613 at 3:9-21.)

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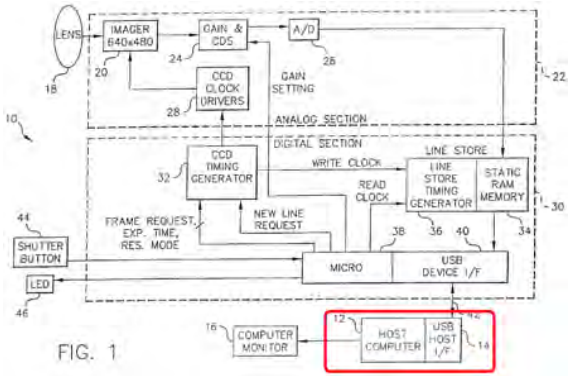
Claims	**Asaida 782**	**in combination with one or more of the following references**
		"The host computer 12 controls the camera picture-taking process by instructing the camera 10 when to take still or motion pictures, and setting the electronic exposure time and the analog gain in the CDS/gain block 24 via the microprocessor 38." (Endsley 613 at 4:60-64.)  FIG. 1 Endsley 613 (Figure 1) "A digital section 30 includes a CCD timing generator 32, a static RAM line store memory 34, a line store timing generator 36, a microprocessor 38, and a USB device interface 40." (Endsley 471 at 3:19-22.) "The output of the line store memory 34 is connected to the host computer 12 via the USB device interface 40, which operates at a maximum data rate of 12M bits/sec. (See the article 'Universal Serial Bus to Simplify PC I/O', by Michael

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		Slater in Microprocessor Report, Volume 9, Number 5, Apr. 17, 1995 for more detail about the benefits of the USB interface.) The USB interface 40, which may be incorporated as part of the microprocessor 38, such as the Intel 82930 microprocessor, reads data from the line store 34." (Endsley 471 at 3:37-46.) "[T]he present invention includes a novel way of 'line throttle clocking' the image sensor 20 by varying a line blanking interval 68 from line to line, as shown in FIG. 5, so as to transfer lines of data from the CCD image sensor 20 into the line store memory 34 at the appropriate time." (Endsley 471 at 4:54-59.) "FIG.5 shows that, once the image data is transferred by the readout pulse 60 to the light-protected vertical registers 50, the line clocking is 'throttled' to accommodate the storage capacity of the line store memory 34. The line store memory 34 is capable of storing a small number of lines of data and provides block transfer capability at low cost. Whenever the line store memory 34 has sufficient room to accommodate a new line of image data, the timing generator 32 creates the vertical and horizontal timing pulses 62 and 64 needed to read out the next line from the image sensor, as shown in FIG. 5, and then returns to a wait state until sufficient data is transferred from the line store memory 34 to the computer 12 so as to provide room for the next line. Since the waiting period (equal to the line blanking time) depends on the USB bus traffic, the line readout times and frame readout times are variable, rather than fixed, as in prior art cameras." (Endsley

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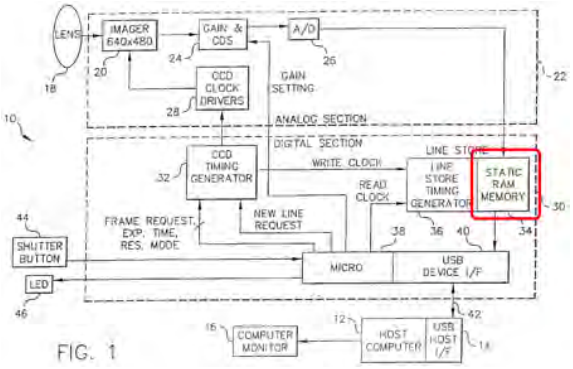
Claims	**Asaida 782**	**in combination with one or more of the following references**
		471 at 4:60-5:9.)  FIG. 1 Endsley 471 (Figure 1) ***Alternatively***, this limitation is met by memory in the USB device interface that contains information related to USB descriptors. "The USB interface 40 . . . may be incorporated as part of the microprocessor 38, such as the Intel 82930 microprocessor." (Endsley 471 at 3:43-45.) "USB devices report their attributes using descriptors. A descriptor is a data structure with a defined format. Each descriptor begins with a byte-wide field that contains the total number of bytes in the descriptor followed by a byte-wide field that identifies the descriptor type. "Using descriptors allows concise storage of the attributes of individual configurations because each configuration may

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		reuse descriptors or portions of descriptors from other configurations that have the same characteristics. In this manner, the descriptors resemble individual data records in a relational database." (USB Spec. Rev. 1.0 at 181.) "A device descriptor describes general information about a USB device. It includes information that applies globally to the device and all of the device's configurations. A USB device has only one device descriptor." (USB Spec. Rev. 1.0 at 182.) "An apparatus sends electrical signals that represent an optical image to a processor for conversion to video signals suitable for display on a display device. The apparatus includes a device for insertion into a region to be viewed for developing an optical image of the region, an imager for generating electrical signals that represent the optical image, and a digital memory for storing information about the imager. The device is adapted to be connected to the processor so that the processor can receive the electrical signals from the imager and obtain information from the digital memory. The processor uses the information from the digital memory in performing the conversion." (Dowdy 082 at Abstract.) "The camera head and endoscope are typically detachable as a unit from the control unit so that a variety of camera heads can be used with a single control unit. This offers a number of advantages. For example, if a first camera head fails, the control unit can be operated with another camera head while

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		the first camera head is being serviced. Also, different types of camera heads, each of which may be most useful for certain procedures, can be used with a single control unit so as to avoid the expense of purchasing and maintaining multiple control units." (Dowdy 082 at 1:25-34 (Background of the Invention).) "In one general aspect, this invention features an apparatus for providing electrical signals that represent an optical image to a processor for conversion to video signals suitable for display on a display device. The apparatus includes a device for insertion into a region to be viewed for developing an optical image of the region, an imager for generating electrical signals that represent the optical image, and a digital memory for storing information about the imager. The device is adapted to be connected to the processor so that the processor can receive the electrical signals from the imager and obtain information from the digital memory. The processor uses the information from the digital memory in performing the conversion." (Dowdy 082 at 1:38-50 (Summary of the Invention).) "The digital memory stores information about the configuration of the imager. This information can include the location of the imager relative to the device. For example, the information identifies whether the imager is located at the distal end or the proximal end of the device. The imager is a charge coupled device. The information identifies an optical format size of the charge coupled device." (Dowdy 082 at 1:53-59.)

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		"The digital memory also stores information about variations in performance characteristics of the imager relative to nominal performance characteristics. When the apparatus includes optics, the information in the digital memory accounts for variations in performance characteristics of the optics relative to nominal performance characteristics. Similarly, when the imager includes a charge coupled device or a cable for connection to the processor, the information accounts for variations in performance characteristics of the charge coupled device or the cable relative to nominal performance characteristics. The information also identifies variations in luminance and color reproduction by the imager." (Dowdy 082 at 1:60-2:5 (Summary of the Invention).) "When the apparatus is designed for application to particular regions, the information identifies characteristics of the region to be viewed by the imager. This allows the processor to optimize the conversion for parameters that are desirable in a particular application." (Dowdy 082 at 2:6-10.) "In one embodiment, the digital memory is a non-volatile storage device, and can be implemented using an EEPROM." (Dowdy 082 at 2:16-17.) "When the information stored in the digital memory identifies the configuration of the device, the processor modifies the conversion based on the configuration. This allows the processor to automatically optimize the

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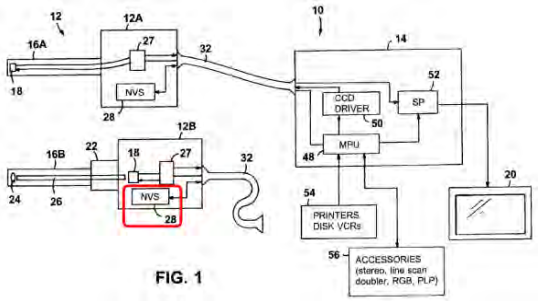
		conversion for different configurations of the device." (Dowdy 082 at 2:34-38.) "Referring also to FIG. 2, to enable different types of camera heads 12 to be used with camera processor 14 without impacting the quality of the video image displayed on video monitor 20, each camera head 12A, 12B (referred to generally with reference numeral 12) includes a non-volatile storage device ("NVS") 28 that stores information identifying the configuration 30 of the particular camera head 12A, 12B. Camera processor 14 uses the information stored in NVS 28 to modify processing of the electrical signals produced by camera head 12, and thereby accounts for the properties of the configuration 30 to which camera head 12 belongs. In a preferred embodiment, NVS 28 is implemented as an electrically erasable programmable read only memory ("EEPROM"). One such EEPROM is an eight pin, 256 byte storage capacity memory available from the Xicor Corp. as model number 24XC02." (Dowdy 082 at 3:62-4:10.)  FIG. 1

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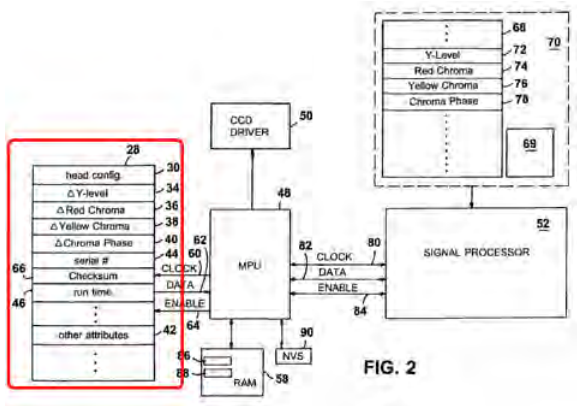
		Dowdy 082 (Figure 1)  FIG. 2 Dowdy 082 (Figure 2) "In addition to variations caused by the configuration of camera head 12, the electrical signals produced by camera head 12 can also vary, because performance characteristics of camera heads 12 tend to vary from device to device. These variations, which are caused primarily by differences in optics, CCDs 18, and cables 32 that are attached to camera heads 12 and connect camera heads 12 to camera processor 14, can adversely affect the ability of a camera head 12 to produce electrical signals that result in an optimal video image. Thus, to further ensure consistent performance when different camera heads 12 are used, NVS 28 also stores information that identifies variations in the performance characteristics of a particular camera head 12 from nominal values." (Dowdy 082 at 4:11-24.)

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		"To enable the video image produced at video monitor 20 to be optimized for certain procedures, the NVS 28 of a camera head 12 designed for those procedures can include information 42 that is used by camera processor 14 to optimize certain signal processing attributes. For example, in a camera head 12 designed for procedures requiring improved edge definition, NVS 28 stores edge enhancement information 42 that replaces nominal edge enhancement values stored within and used by camera processor 14. Similarly, in camera heads 12 designed for procedures in which the white or grey brightness ranges are of particular interest, NVS 28 stores information 42 that modifies, respectively, operation of the so-called "knee circuit" (which implements a nonlinear function for compressing, rather than clipping, the upper level, white, component of the video signal) and the operation of the so-called "gamma circuit" (which implements a nonlinear function for optimizing the median level, grey, component of the video signal) implemented by signal processor 14." (Dowdy 082 at 4:36-54.) "For servicing and other purposes, NVS 28 also stores information that identifies the serial number 44 of camera head 12 and a measure 46, in minutes and hours, of the run time that camera head 12 has experienced." (Dowdy 082 at 4:55-58.) "Referring also to FIG. 3, MPU 48 uses the information stored in NVS 28 to control the operation of CCD driver 50

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		and signal processing circuitry 52. When the user connects cable 32 of camera head 12 to camera processor 14, and, if necessary, powers up video endoscopy system 10, MPU 48 detects the connection and responds by downloading the information from NVS 28 into a memory 58, such as a RAM, of MPU 48 (step 200). MPU 48 reads the stored information out of NVS 28 through a serial data link in cable 32 that includes a CLOCK line 60 controlled by MPU 48 and a DATA line 62 that is shared by NVS 28 and MPU 48." (Dowdy 082 at 5:9-19.) "Referring to FIG. 4, in a more detailed view, camera head 12 includes CCD 18 (located, as discussed, either in the head or at the tip of the endoscope), NVS 28 and a set of button switches 92 for system control, and camera processor 14 includes a camera controller 94 and a signal processor 96. Cable 32, which connects camera head 12 to camera processor 14, carries drive signals from CCD driver 50 in signal processor 96, electrical signals from CCD 18 to a preamplifier 98 in signal processor 96, data between NVS 28 and MPU 48 in camera controller 94, and signals from button switches 92 to MPU 48." (Dowdy 082 at 6:48-58.)

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		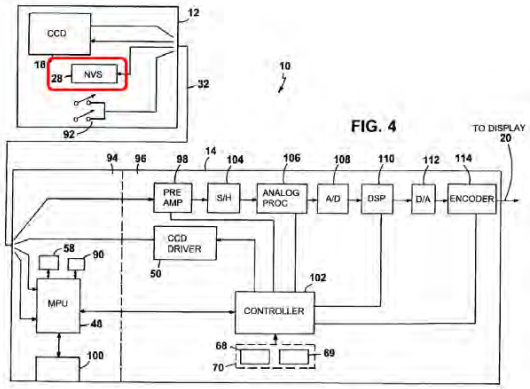 Dowdy 082 (Figure 4) "MPU 48 controls signal processor 96 in response to signals from button switches 92 and signals from controls in a front panel 100 of camera controller 94. The controls in front panel 100 allow the user of video endoscopy system 10 to configure button switches 92 to perform desired functions. Thus, for example, button switches 92 could be configured to cause signal processor 96 to pause the video image displayed at video monitor 20 (FIG. 1). MPU 48 also displays system parameters at front panel 100, interacts with NVS 28 by downloading information about camera head 12 and updating run time information in NVS 28, updates signal processing parameters in light of the information about camera head 12, and communicates with signal processor 96, all as discussed above." (Dowdy at 6:59-7:5.) "A nonvolatile, programmable memory is incorporated in an

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		endoscope. Endoscope-related data closely relevant to the endoscope, such as, an endoscope model name and the number of power feeds are stored in the nonvolatile memory. The endoscope is connected to an external image processing apparatus, and endoscope-related data is read from the nonvolatile memory. Based on the read endoscope-related data, the use situation of the endoscope is grasped or the endoscope is managed. The number of power feeds is varied depending on the use situation of the endoscope, and written in the nonvolatile memory. Thus, the endoscope-related data is used to maintain the endoscope and reduce a load to be incurred by the external image processing apparatus that is a connected apparatus. Consequently, the endoscope can be managed and maintained easily using a small software system." (Oshima 212 at Abstract.) "[An] object of the present invention is to provide an endoscope system in which endoscope-related data including a use situation of an endoscope can be checked readily." (Oshima 212 at 1:60-62.) "A regulator 19, a programmable nonvolatile memory 20, a CPU 21, a selector (SEL) 22, a supply voltage detector 23, a scope switch 24, and a connector 25 are arranged behind the rear end of the insertion unit 11 of the endoscope 2. The regulator 19 converts a CCD driving voltage fed from a CCD driving power supply 18 incorporated in the image processing apparatus 3A into a desired voltage. The programmable nonvolatile memory 20 in which the endoscope-related data is stored is realized with an

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		EEPROM, a flash ROM, an FRAM, or an MRAM." (Oshima 212 at 6:54-63.) "Especially important data out of endoscope-related data storable in the nonvolatile memory 20 includes, for example, an endoscope model name, the structure of the distal part of an endoscope, a cleaning tube/adaptor name, a CCD model name, a type of optical filter in a CCD, information relating to the channels in an endoscope, information relating to the switches on an endoscope, a version number, and identification data." (Oshima 212 at 29:16-25.)

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		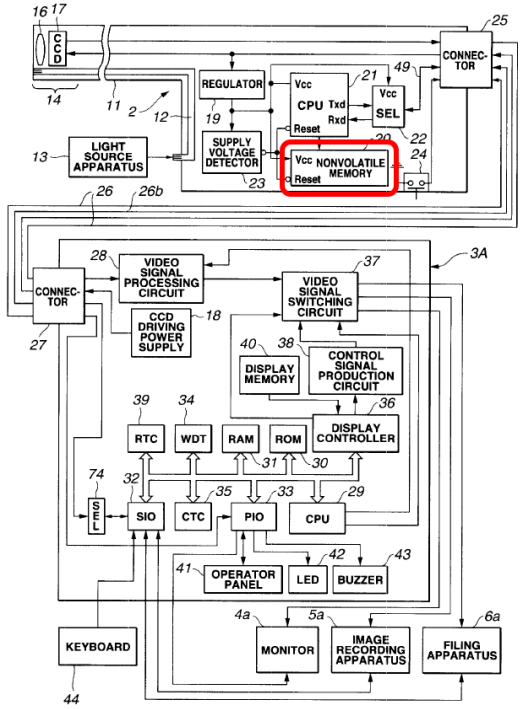 Oshima 212 (Figure 2) "FIG. 35 describes processing to be performed in the image processing apparatus 3A, which has the ability to communicate with the endoscope 2 and is connected to the endoscope 2, for treating count data contained in data to be stored in the nonvolatile memory 20 in the endoscope 2." (Oshima 212 at 29:59-63.)

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		"The connected apparatus 3A uses connection sensing means (not shown) incorporated in the endoscope and the connected apparatus to judge whether it has been connected to the endoscope 2 (S321). If connection is sensed, identification data or an endoscope model name is read first (S322)." (Oshima 212 at 29:66-30:4.) "From the foregoing description of the prior art, it is clear that the 'bad pixel' data is never transferred to the camera portion, but instead remains in the local controller memory. Accordingly if a camera has been subjected to pixel evaluation for existence of blemishes using a CCU with a blemish compensating capacity as described above, another camera cannot be used in its place with the same CCU unless the CCU blemish compensator is again operated to evaluate the pixels of the new camera. Moreover, assuming that blemish compensation is desired, a camera that has been evaluated by the CCU of Fig. 1 is not interchangeable with another like blemish compensator-equipped CCU unless it is first re-evaluated for blemishes." (Zu 391 at 5-6.) "This non-interchangeability of cameras with a CCU is especially limiting in the case of video endoscopes. During surgery, it may be necessary to employ two or more video endoscopes when only one CCU may be available. With a compensator-equipped CCU as shown in Fig. 1, substitution of one video camera endoscope for another may be frustrated by the need to first evaluate the camera for blemishes and record the 'bad pixels' in the CCU's digital memory so that compensation may be accomplished when video information

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		is acquired by the endoscope's camera." (Zu 391 at 6.) "The object of this invention is to facilitate use of video cameras having known pixel blemishes with different camera control units." (Zu 391 at 6.) "The present invention comprises incorporating into a CCD-type video camera an electronically programmable non-volatile memory which stores the location of 'bad' pixels and is controlled by a device which is located remotely from the camera in a separate CCU. This arrangement assures that video cameras are interchangeable with CCU's regardless of CCD blemish content." (Zu 391 at 6.) "Fig. 2 illustrates the invention. Except as described hereinafter, the system shown in Fig. 2 incorporates the same elements and the same functions as the system of Fig. 1, and identical elements are identified by the same numerals. In this case, the camera 2 is modified by incorporating therein an electronically programmable non-volatile digital memory 42 which is coupled to camera connector 14 via a suitable bus 44." (Zu 391 at 7.)

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		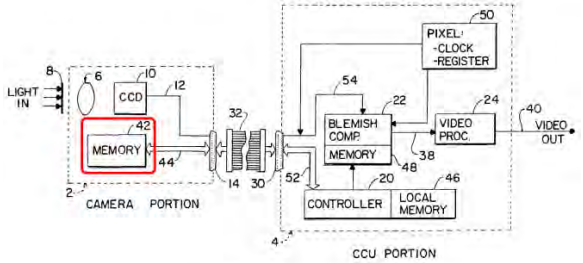 FIG. 2 Zu 391 (Figure 2) "In the operational mode, the data in memory 42 is transferred to memories 46 and 48 whenever the unit is energized. The blemish compensation operation is then performed by the blemish compensator 22 using pixel address data downloaded from camera memory 42. The pixel address data is downloaded from camera memory 42 to blemish compensator memory 48 by the controller 20 via the buses 44 and 52." (Zu 391 at 8.) "When the operational mode is initiated with the camera coupled to a CCU 4 as described, the controller 22 downloads the pixel address data from the camera's memory 42 to the protected local memory 46 of the controller 20. Subsequently that data is loaded into the volatile memory 48 of the blemish compensator 22. Typically this data transfer from camera memory 42 t the local memory 46 of the controller occurs after a forced rest imposed by controller 20, which clears, resets, and reloads all non-protected CCU

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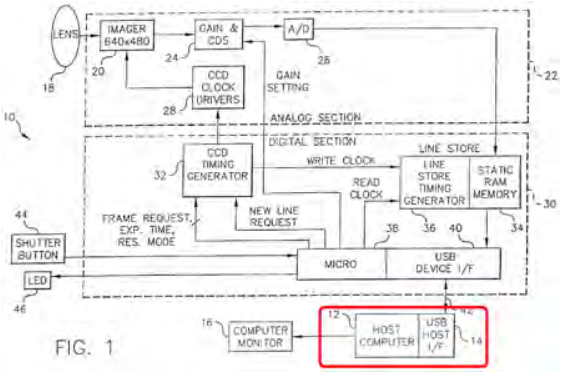
		memory." (Zu 391 at 9.)
16. The video imaging system according to claim 15 wherein said camera head further comprises a multiplexer, for generating a multiplexed signal, which includes the digital image signal and control signals.	*See* Claim 15. The analysis of claim 15 is incorporated by reference in its entirety. "The multiplexor 18 is supplied with control data D_{CTL} from a synchronizing circuit block 19 and a control circuit block 20, while being supplied with voice data D_{MIC}, from a microphone signal inputted from a microphone input terminal 21 by means of a selector 22 and digitized by an A/D converter 23 into audio data $D_{MIC/AUDIO}$. The multiplexor 18 adds the signals D_{CTL} and $D_{MIC/AUDIO}$ to a digital video signal D_{VIDEO} composed of the digital component Video signals D_Y, D_{CR} and D_{CB} or the digital composite video signal D_{CS} supplied from the encoder 14. Output data D_{MPX} from the multiplexor 18, that is, the digital video signal D_{VIDEO} added to the control data D_{CTL} and the audio data $D_{MIC/AUDIO}$, are outputted in parallel at a parallel output port 24, while being converted by P/S converter 25 from parallel data into serial data which are serially outputted at a serial output port 26." (Asaida 782 at 6:67-7:15.)	"The camera 10 is connected to a host computer 12 via a USB (universal serial bus) digital host interface 14, which also provides power to the camera 10. . . . The camera 10 can acquire both still and motion images. The camera data is processed by the host computer 12 to create final images that can be displayed on a computer monitor 16, e.g., transmitted along with audio as part of a "computer videoconference", etc." (Endsley 613 at 3:9-21.) "The host computer 12 controls the camera picture-taking process by instructing the camera 10 when to take still or motion pictures, and setting the electronic exposure time and the analog gain in the CDS/gain block 24 via the microprocessor 38." (Endsley 613 at 4:60-64.)  Endsley 613 (Figure 1)

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	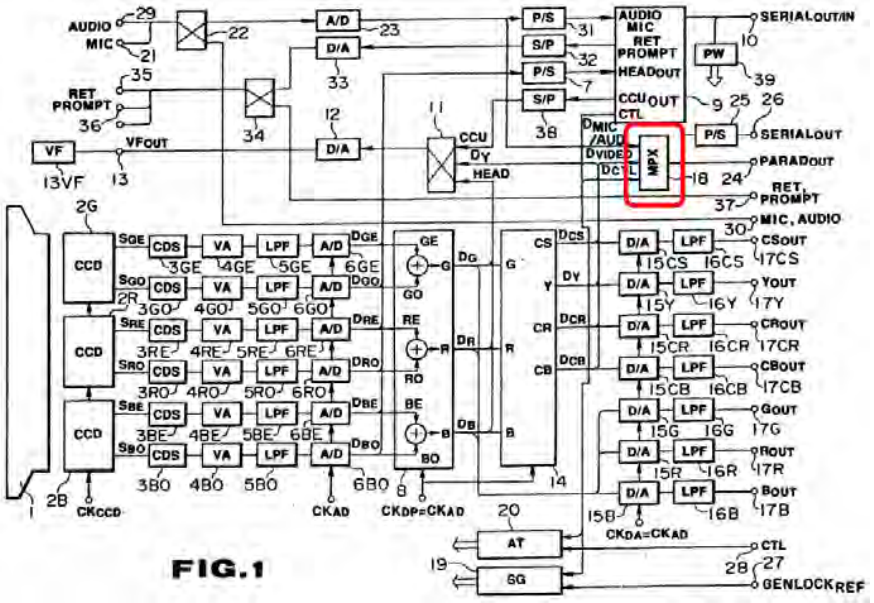 FIG.1 Asaida 782 (Figure 1)	
19. The video imaging system according to claim 15 wherein said camera head utilizes at least one	*See* Claim 15. The analysis of Claim 15 is incorporated by reference in its entirety. Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005) (citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)).	"Reference is now made to FIG. 4, which is an schematic block diagram of the miniature endoscope according to a preferred embodiment of the present invention. Parts that are identical to those shown above are given the same reference numerals and are not referred to again except as necessary for an understanding of the present embodiment. Optical assembly 48 receives light, indicated by arrows 60, from an object being viewed. The light is processed by optical assembly 48, as will be explained below, to reach image sensor 46 were it is converted from photons into electrical

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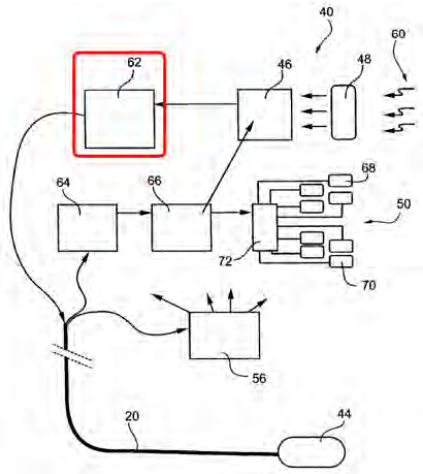
digital serial driver utilizing Low-Voltage Differential Signals.	Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	signals. The electrical signals are digitized and passed to a transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Adler 940 at 10:7-19.)  Adler 940 (Figure 4) "Figure 1 shows a typical connection with LVDS drivers and receivers."

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		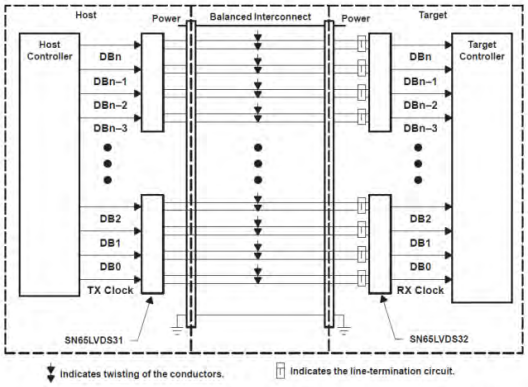 Figure 1. Typical Connection With LVDS Drivers and Receivers TI LVDS (Figure 1) "The LVDS driver produces a differential voltage across a 100-Ω load in the range of 247 mV to 454 mV with a typical offset voltage of 1.2 V relative to ground (see Figure 2). Most drivers are commonly imple3mented as current-mode devices, which allow frequency to be virtually independent of power consumption. These two characteristics, low voltage swings and constant current, allow LVDS drivers to operate at higher data rates and lower power dissipation." (TI LVDS at 2.) "As the need for higher bandwidth accelerates, system designers are choosing differential signaling to satisfy high bandwidth requirements while reducing power, increasing noise immunity, and decreasing EMI emissions. LVDS is a low swing, differential signaling technology providing very

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		fast data transmission, common-mode noise rejection, and low power consumption over a broad frequency range. The Virtex-E family delivers the programmable industry's highest bandwidth and most flexible differential signaling solution for direct interfacing to industry-standard LVDS devices." (Virtex-E LVDS at 1.) "With up to 36 I/O pairs operating at 622 Megabits per second (Mb/s) or up to 344 I/O pairs operating at over 311 Mb/s, the Virtex-E family supports multiple 10 Gb/s ports while maintaining high signal integrity with low power consumption. Unlike other PLD solutions, all Virtex-E LVDS I/Os support input, output, and I/O signaling, providing a system designer unparalleled flexibility in board layout." (Virtex-E LVDS at 1.) Advantages of LVDS include: "• LVDS is specified to be technology and process independent. • LVDS is EMI tolerant. Common-mode noise is equally removed by two conductors and rejected by the receiver. • No transmission medium is defined in the standard. The medium can be tailored to meet the specific application requirements. • The typical LVDS voltage swing is 350 mV, resulting in a higher transfer rate and lower power consumption." (Virtex-E LVDS at 2.) "There are two configurations that are used in LVDS applications, point-to-point and multi-drop. The Virtex-E

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		family supports both LVDS configurations. **Point-to-Point** In point-to-point configuration, there is one transmitter and one receiver. The LVDS driver is a current source that drives a differential pair of lines. The typical current drive is 3.5 mA. The receiver has high DC impedance. The majority of the driver current flows across the termination resistor generating about 350 mV at the receiver inputs (Figure 1). **Multi-Drop** A multi-drop LVDS configuration has one transmitter and multiple receivers. The differential termination resistor is placed close to the last receiver (Figure 3)." (Virtex-E LVDS at 2.) Among the many applications that LVDS is suited for are "digital cameras" and "multimedia peripherals." (Virtex-E LVDS at 2-3.) "Figure 1 shows the schematic of a standard LVDS driver driving the Virtex-E receiver. An LVDS driver drives the two 50 W transmission lines into a Virtex-E LVDS receiver. The two 50 W single-ended transmission lines can be micro-strip, strip-line, a 100 W differential twisted pair, or a similar balanced differential transmission line." (Virtex-E LVDS at 3.)

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		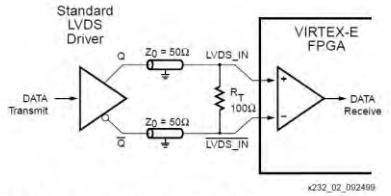 Figure 1: A Standard LVDS Driver Driving a Virtex-E LVDS Receiver <u>Virtex-E LVDS (Figure 1)</u> "As may be seen, the circuit of FIG. 4 employs a plurality of LVDS circuits 11. Each circuit 11 includes a respective driver 54 and a respective receiver 56. Each driver 54 receives a respective input signal Din0, Din1 . . . Dinn, which are digital logic levels of, for example, 3.3 volts for logic "1" and zero volts for logic "0". Changes in state in these signals are transmitted over the differential lines to the respective receivers 56. Each receiver 56 generates a respective output signal Dout0, Dout1, . . . Doutn, which are at the several hundred millivolt level." (Chung 290 at 2:27-36.)

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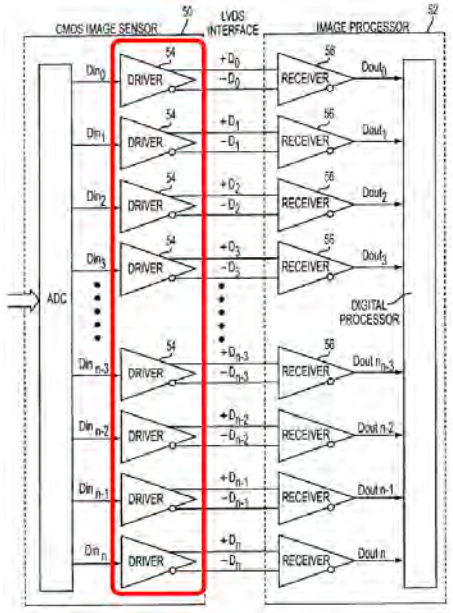
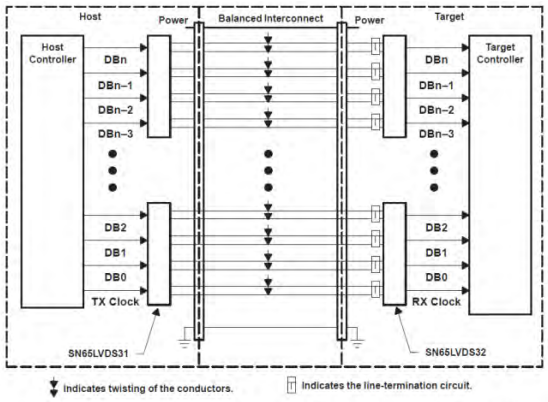
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Chung 290 (Figure 4)
20. The video imaging system according to claim 15 wherein said camera control unit utilizes at	*See* Claim 20. The analysis of Claim 20 is incorporated by reference in its entirety. Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005) (citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)).	"Reference is now made to FIG. 4, which is an schematic block diagram of the miniature endoscope according to a preferred embodiment of the present invention. Parts that are identical to those shown above are given the same reference numerals and are not referred to again except as necessary for an understanding of the present embodiment. Optical assembly 48 receives light, indicated by arrows 60, from an object being viewed. The light is processed by optical assembly 48, as will be explained below, to reach image sensor 46 were it is converted from photons into electrical

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
least one digital serial receiver utilizing Low-Voltage Differential Signals.	Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	signals. The electrical signals are digitized and passed to a transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Adler 940 at 10:7-19.) If the electrical signals are transmitted to the processing device 30 using an LVDS transmitter, the at least one digital serial receiver in the processing device that receives the signals must necessarily utilize Low-Voltage Differential Signals. "Figure 1 shows a typical connection with LVDS drivers and receivers."  Figure 1. Typical Connection With LVDS Drivers and Receivers TI LVDS (Figure 1)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		"The recommended voltage applied to the receiver is between ground and 2.4 V with a common mode range of 0.2 V to 2.2 V. The receiver has a sensitivity level of ±100 mV to correctly assume the intended binary state (see Figure 2). The LVDS interconnecting media must be matched with the 100-Ω termination resistor located at the inputs of the receiver." (TI LVDS at 4.) "There are two configurations that are used in LVDS applications, point-to-point and multi-drop. The Virtex-E family supports both LVDS configurations. **Point-to-Point** In point-to-point configuration, there is one transmitter and one receiver. The LVDS driver is a current source that drives a differential pair of lines. The typical current drive is 3.5 mA. The receiver has high DC impedance. The majority of the driver current flows across the termination resistor generating about 350 mV at the receiver inputs (Figure 1). **Multi-Drop** A multi-drop LVDS configuration has one transmitter and multiple receivers. The differential termination resistor is placed close to the last receiver (Figure 3)." (Virtex-E LVDS at 2.) Among the many applications that LVDS is suited for are "digital cameras" and "multimedia peripherals." (Virtex-E LVDS at 2-3.)

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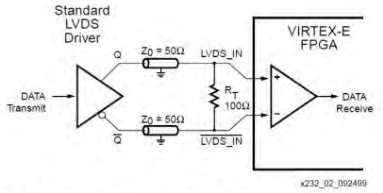
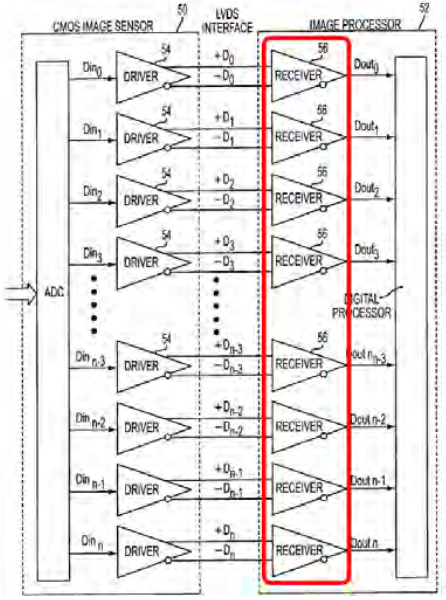
Claims	**Asaida 782**	**in combination with one or more of the following references**
		"Figure 1 shows the schematic of a standard LVDS driver driving the Virtex-E receiver. An LVDS driver drives the two 50 W transmission lines into a Virtex-E LVDS receiver. The two 50 W single-ended transmission lines can be micro-strip, strip-line, a 100 W differential twisted pair, or a similar balanced differential transmission line." (Virtex-E LVDS at 3.)  **Figure 1: A Standard LVDS Driver Driving a Virtex-E LVDS Receiver** Virtex-E LVDS (Figure 1) "As may be seen, the circuit of FIG. 4 employs a plurality of LVDS circuits 11. Each circuit 11 includes a respective driver 54 and a respective receiver 56. Each driver 54 receives a respective input signal Din0, Din1 . . . Dinn, which are digital logic levels of, for example, 3.3 volts for logic "1" and zero volts for logic "0". Changes in state in these signals are transmitted over the differential lines to the respective receivers 56. Each receiver 56 generates a respective output signal Dout0, Dout1, . . . Doutn, which are at the several hundred millivolt level." (Chung 290 at 2:27-36.)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Chung 290 (Figure 4)
21. A video imaging system comprising:	To the extent the preamble is limiting, Asaida 782 discloses "[a] video imaging system." "This invention relates to a video camera forming digital signals representing an object projected on an imaging device and, more particularly, to a video camera having a signal processing circuit for performing digital signal processing on output signals of the imaging device." (Asaida 782 at 1:7-12.) "FIG. 1 is a block diagram showing an embodiment of a camera head	To the extent the preamble is limiting, Okada 852 discloses "[a] video imaging system." "The present invention relates to an imaging device for an endoscope, and more particularly, it relates to the composition of an endoscope system which can display a picture imaged by using one scope, by either system selected from the NTSC system and the PAL system." (Okada 852 at 1:12-16."

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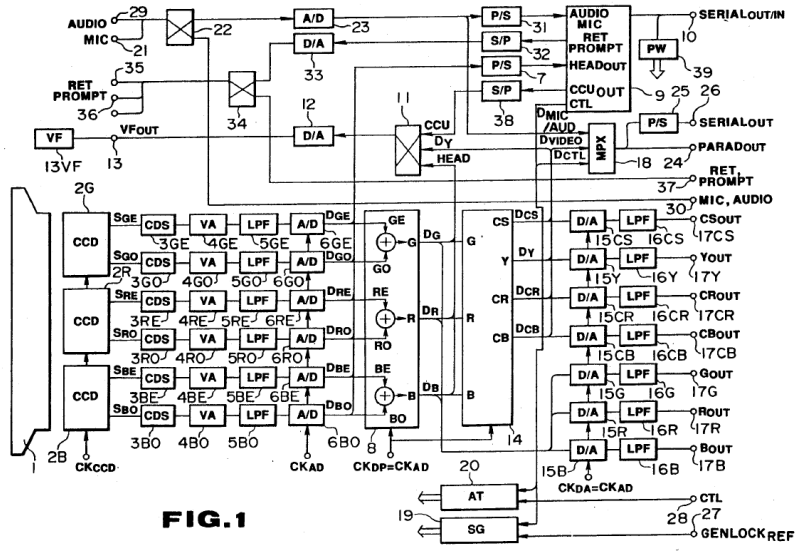
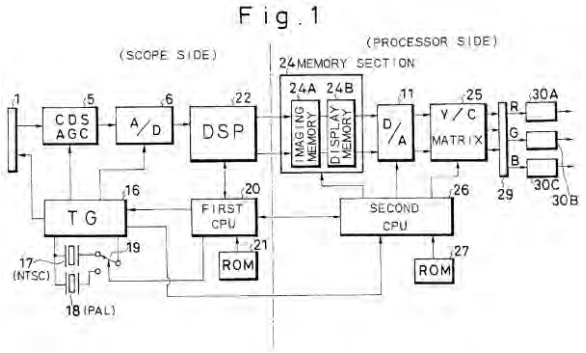
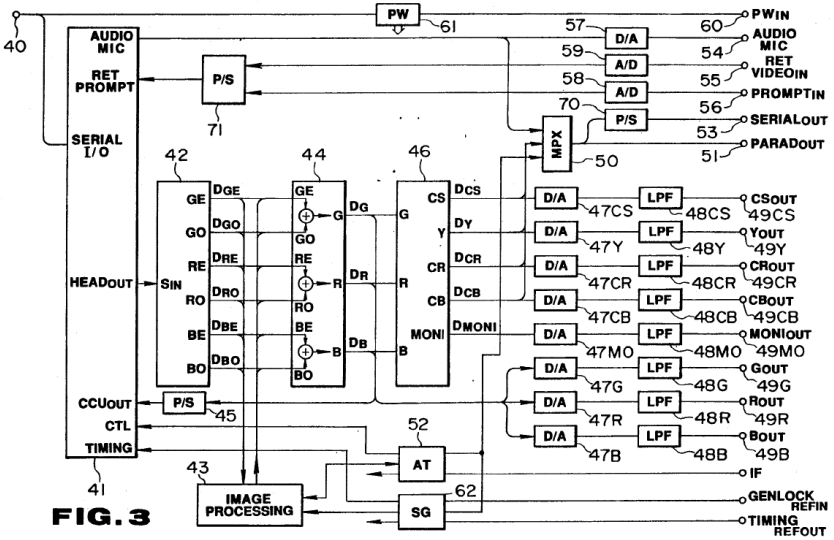
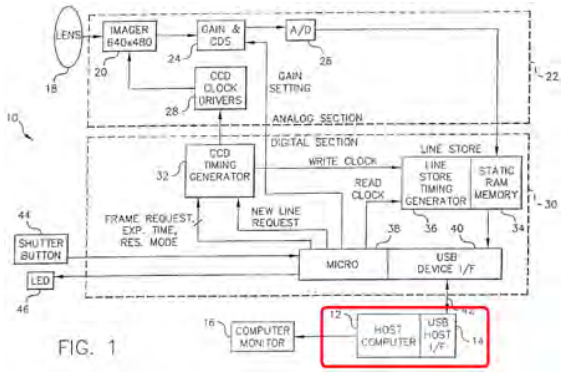
Claims	**Asaida 782**	**in combination with one or more of the following references**
	unit of a video camera according to the present invention." (Asaida 782 at 3:44-46.)  FIG.1 Asaida 782 (Figure 1) "FIG. 3 is a block diagram showing an embodiment of a camera control unit of the video camera shown in FIG. 1." (Asaida 782 at 3:50-52.)	"FIG. 1 is a block diagram showing the circuit configuration of an electronic endoscope equipped with both the NTSC system and the PAL system according to an embodiment of the present invention." (Okada 852 at 3:58-61.)  Okada 852 (Figure 1) "The camera 10 is connected to a host computer 12 via a USB (universal serial bus) digital host interface 14, which also provides power to the camera 10. . . . The camera 10 can acquire both still and motion images. The camera data is processed by the host computer 12 to create final images that can be displayed on a computer monitor 16, e.g., transmitted along with audio as part of a "computer videoconference", etc." (Endsley 613 at 3:9-21.) "The host computer 12 controls the camera picture-taking process by instructing the camera 10 when to take still or

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
	 FIG. 3 Asaida 782 (Figure 3)	motion pictures, and setting the electronic exposure time and the analog gain in the CDS/gain block 24 via the microprocessor 38." (Endsley 613 at 4:60-64.)  Endsley 613 (Figure 1) To the extent the preamble is limiting, Endsley 471 discloses a video imaging system. Specifically, "[a] block diagram of a digital imaging system according to the invention is shown in FIG. 1. The system includes a camera 10 connected to a host computer 12 via a USB (universal serial bus) cable 42 connected to a USB digital host interface 14, which also provides power to the camera 10. . . . The camera 10 can acquire both still and motion images." (Endsley 471 at 2:49-59.)

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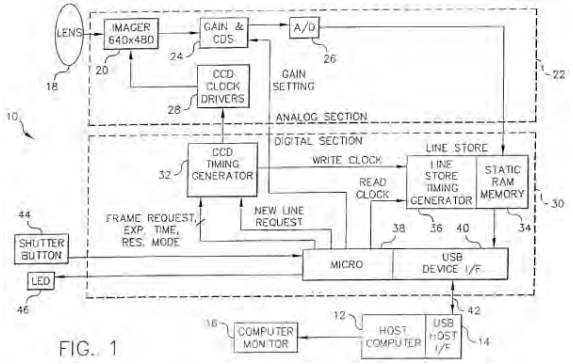
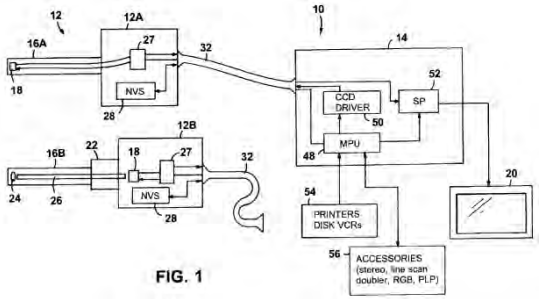
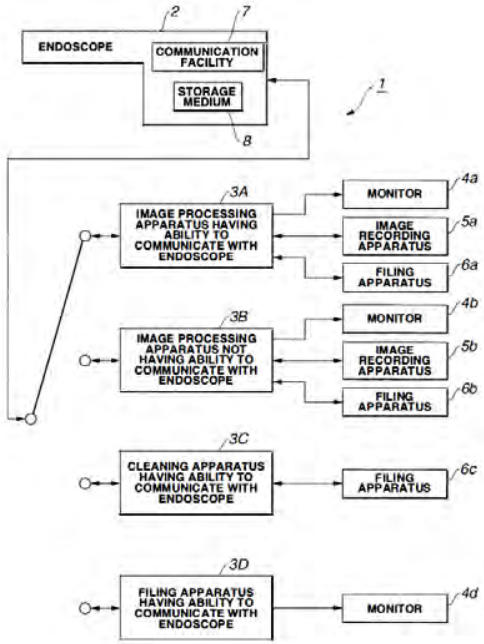
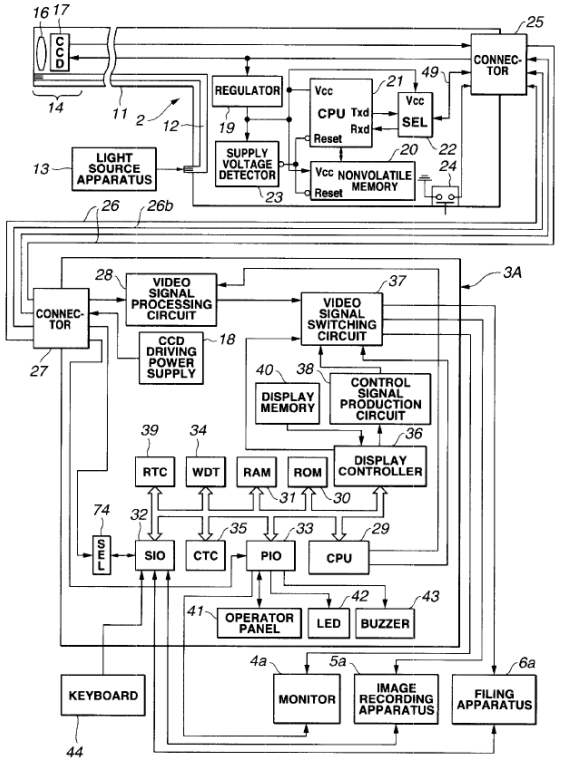
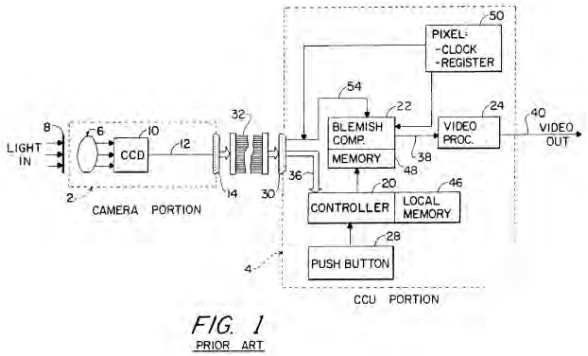
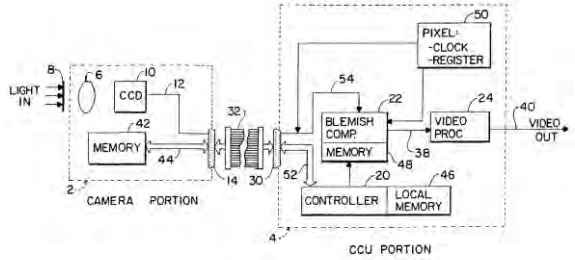
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Endsley 471 (Figure 1) To the extent the preamble is limiting, Dowdy 082 discloses "[a] video imaging system." "The invention relates to camera heads for use with remote video display systems such as video endoscopy systems, borescopes, and other devices." (Dowdy 082 at 1:10-12.) "Referring to FIG. 1, a video endoscopy or borescope system 10 includes a camera head 12 and a camera processor 14. Camera head 12 includes an endoscope 16 for insertion into a region such as a body cavity, and an imaging device, such as a CCD 18, that produces electrical signals representative of an optical image at the distal end of endoscope 16. Camera processor 14 processes the electrical signals produced by camera head 12 to generate a video image that is displayed on a video monitor 20." (Dowdy 082 at 3:24-32.)

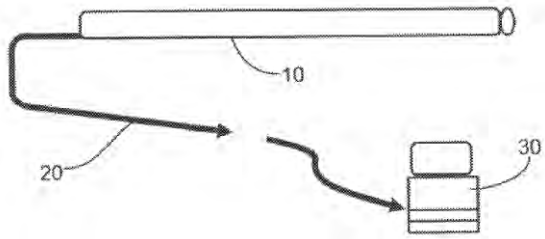
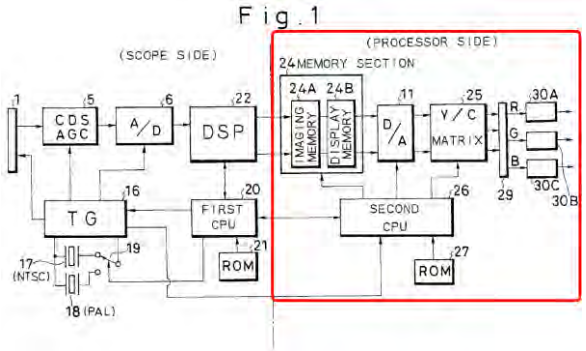
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 FIG. 1 Dowdy 082 (Figure 1) To the extent the preamble is limiting, Oshima 212 discloses "[a] video imaging system. "An endoscope system 1 in accordance with the first embodiment of the present invention shown in FIG. 1 consists broadly of an endoscope 2, and connected apparatuses (or peripheral equipment) to be selectively connected to the endoscope. The connected apparatuses include an image processing apparatus 3A, an image processing apparatus 3B, a cleaning apparatus 3C, a filing apparatus 3D, a monitor 4 a, an image recording apparatus 5 a, a filing apparatus 6 a, a monitor 4 b, an image recording apparatus 5 b, a filing apparatus 6 b, a filing apparatus 6 c, and a monitor 4 d. The image processing apparatus 3A has the ability to communicate with the endoscope 2. . . ." (Oshima 212 at 5:15-26.)

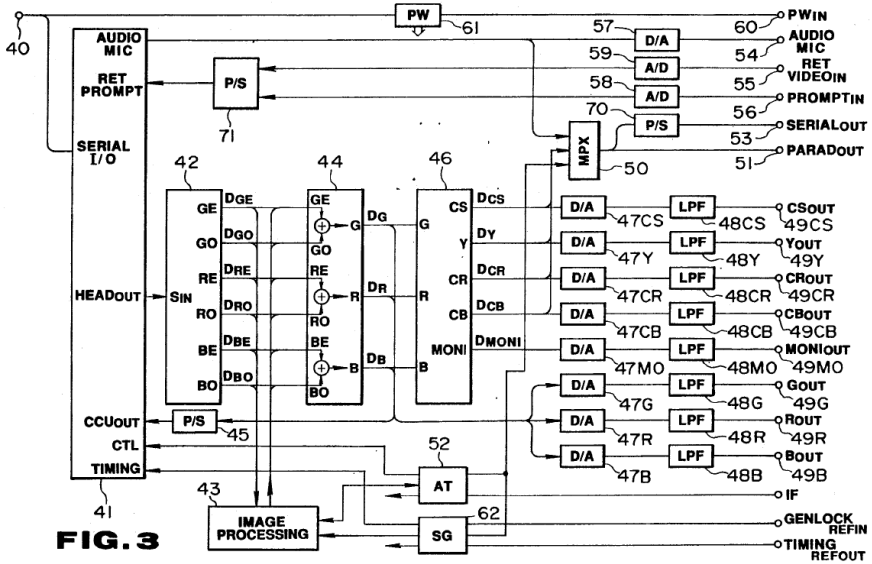
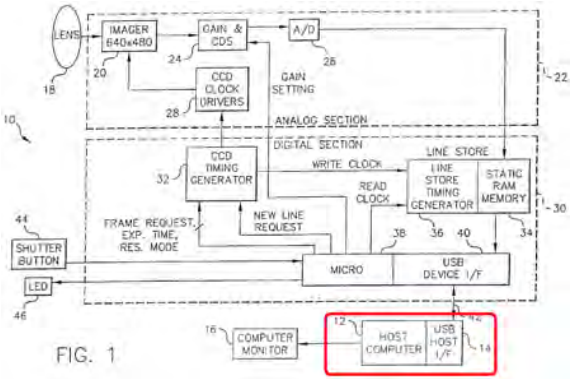
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Oshima 212 (Figure 1) "FIG. 2 is a block diagram showing in detail the endoscope 2 and the image processing apparatus 3A having the communicating ability which are employed in the present embodiment." (Oshima 212 at 6:34-37.)

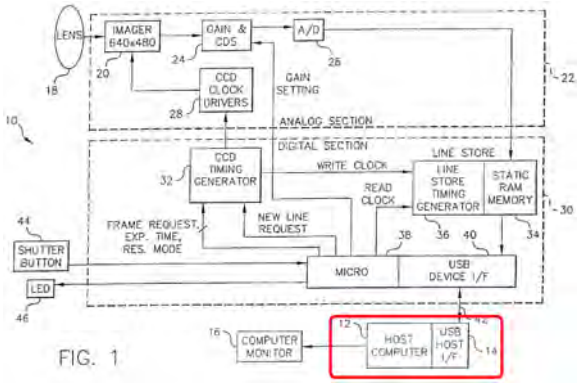
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Oshima 212 (Figure 2) To the extent the preamble is limiting, Zu 391 discloses "[a] video imaging system." "This invention relates to compensating for CCD blemishes in video cameras and ore particularly to cameras that are designed to be used interchangeably with camera control

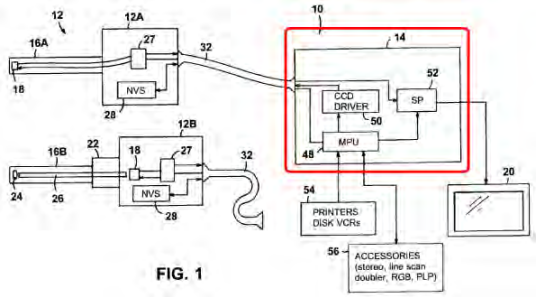
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		units, notably but not exclusively video cameras that are incorporated in endoscopes for use with medical imaging systems." (Zu 391 at 1.) "Fig. 2 illustrates the invention. Except as described hereinafter, the system shown in Fig. 2 incorporates the same elements and the same functions as the system of Fig. 1, and identical elements are identified by the same numerals." (Zu 391 at 7.)  FIG. 1 PRIOR ART Zu 391 (Figure 1)

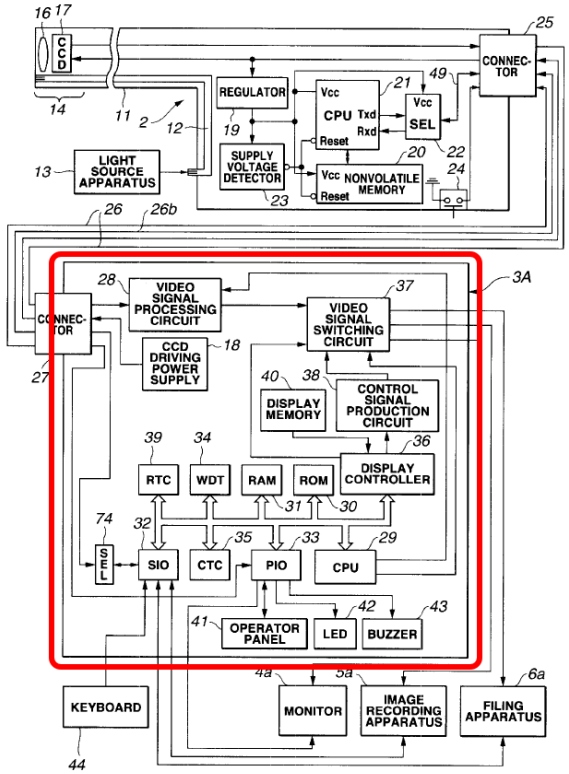
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 FIG. 2 Zu 391 (Figure 2) To the extent the preamble is limiting, Adler 940 discloses "[a] video imaging system." "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope. The skilled person will appreciate that the wire connection 20 may be an optical connection or may instead use RF or a like means of wireless communication. The miniature endoscopic front-end 10 may be designed for connection to any standard PC input (the USB input for example)." (Adler 940 at 9:24-38.)

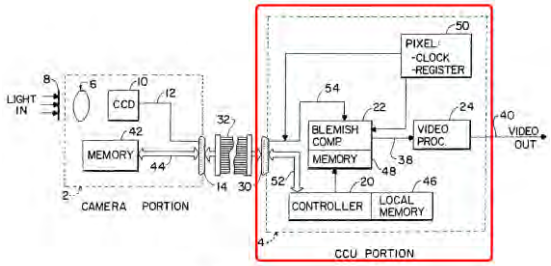
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Adler 940 (Figure 1)
a camera control unit processing a continuous stream of digital video data;	"FIG. 3 is a block diagram showing an embodiment of a camera control unit of the video camera shown in FIG. 1." (Asaida 782 at 3:50-52.) "The video camera according to the present invention is constituted by the above mentioned camera head unit shown in FIG. 1 and the camera control unit CCU arranged and constituted as shown in FIG. 3." (Asaida 782 at 8:1-4.) "The camera control unit CCU, constituting part of the video camera according to the present invention, is provided with a serial input/output port 40, as shown in FIG. 3, which is connected to the serial input/output port 10 of the camera head unit by an optical fiber cable, not shown, constituting transmission means." (Asaida 782 at 8:5-10.)	"[O]n the external processor side, a memory section 24 equipped with an imaging memory 24A and a display memory 24B, a D/A converter 11, a brightness/color signal (Y/C) matrix circuit 25, a second CPU 26 for controlling these circuits, and a ROM 27 storing the setting data for the control meeting the selected television system of the NTSC or the PAL are provided." (Okada 852 at 4:34-40.) 

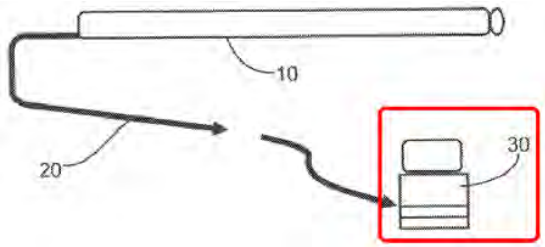
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
	 FIG. 3 Asaida 782 (Figure 3)	Okada 852 (Figure 1) "The camera 10 is connected to a host computer 12 via a USB (universal serial bus) digital host interface 14, which also provides power to the camera 10. . . . The camera 10 can acquire both still and motion images. The camera data is processed by the host computer 12 to create final images that can be displayed on a computer monitor 16, e.g., transmitted along with audio as part of a "computer videoconference", etc." (Endsley 613 at 3:9-21.) "The host computer 12 controls the camera picture-taking process by instructing the camera 10 when to take still or motion pictures, and setting the electronic exposure time and the analog gain in the CDS/gain block 24 via the microprocessor 38." (Endsley 613 at 4:60-64.)  FIG. 1 Endsley 613 (Figure 1)

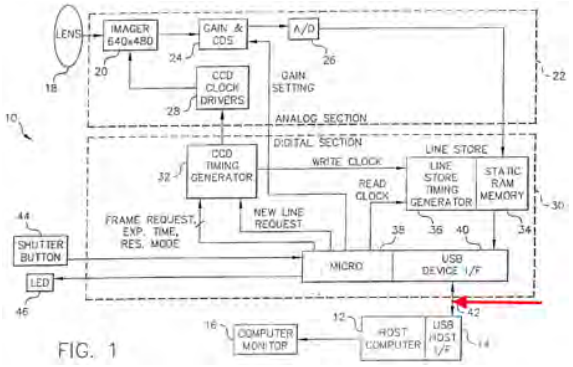
U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		"The system includes a camera 10 connected to a host computer 12 via a USB (universal serial bus) cable 42 connected to a USB digital host interface 14, which also provides power to the camera 10. . . . The camera 10 can acquire both still and motion images. The camera data is processed by the host computer 12 to create final images that can be displayed on a computer monitor 16, e.g., transmitted along with audio as part of a 'computer videoconference', etc." (Endsley 471 at 2:50-63.) "The host computer 12 controls the camera operation. It can instruct the camera 10 when to take still or motion pictures, and set the electronic exposure time via the CCD timing generator 32, and set the analog gain in the CDS/gain block 24 from the microprocessor 38." (Endsley 471 at 3:54-58.)  FIG. 1 Endsley 471 (Figure 1)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		"Referring to FIG. 1, a video endoscopy or borescope system 10 includes a camera head 12 and a camera processor 14. Camera head 12 includes an endoscope 16 for insertion into a region such as a body cavity, and an imaging device, such as a CCD 18, that produces electrical signals representative of an optical image at the distal end of endoscope 16. Camera processor 14 processes the electrical signals produced by camera head 12 to generate a video image that is displayed on a video monitor 20." (Dowdy 082 at 3:24-32.)  FIG. 1 Dowdy 082 (Figure 1) "FIG. 2 is a block diagram showing in detail the endoscope 2 and the image processing apparatus 3A having the communicating ability which are employed in the present embodiment." (Oshima 212 at 6:34-37.)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Oshima 212 (Figure 2) "The image processing apparatus 3A consists broadly of a CCD driving power supply 18, a video signal processing circuit 28, a CPU 29, a ROM 30, a RAM 31, a serial controller (S10) 32, a parallel communication controller (PIO) 33, a watchdog timer (WDT) 34, a counter timer

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		(CTC) 35, a display controller 36, a display memory 40, a video signal switching circuit 37, a control signal production circuit 38, a real-time clock (RTC) 39, an operator panel 41, an LED 42, a buzzer 43, and a light adjustment control unit. The CCD driving power supply 18 applies a voltage to the CCD 17 in the endoscope 2. The video signal processing circuit 28 processes a video signal resulting from photoelectric conversion performed by the CCD 17. The CPU 29 carries out a plurality of arithmetic operations." (Oshima 212 at 7:15-27.) "Figure 1 illustrates a prior art video system comprising a camera 2 and a CCU 4. . . . The CCU 4 comprises a controller 20 with local non-volatile digital memory 46, a blemish compensator 22 with associated volatile digital memory 48, a video signal processor 24, a pixel clock/pixel address register 50, a push-button interface and mode selector 28 for directing operation of controller 20." (Zu 391 at 3.)  FIG. 2

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		Zu 391 (Figure 2) "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope." (Adler 940 at 9:24-33.) "The software included with processing device 30 processes the output of the miniature endoscopic front-end 10. The software may typically control transfer of the images to the monitor of the PC 30 and their display thereon including steps of 3D modeling based on stereoscopic information as will be described below, and may control internal features of the endoscopic front end 10 including light intensity, and automatic gain control (AGC), again as will be described below." (Adler 940 at 9:39-47.) 

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		Adler 940 (Figure 1)
a cable, connected to said camera control unit, for transmitting the stream of digital video data to said camera control unit; and	"The camera control unit CCU, constituting part of the video camera according to the present invention, is provided with a serial input/output port 40, as shown in FIG. 3, which is connected to the serial input/output port 10 of the camera head unit by an optical fiber cable, not shown, constituting transmission means." (Asaida 782 at 8:5-10 (emphasis added).)	"The USB device interface 40 connects to the USB host interface 14 by means of a USB cable 42." (Endsley 613 at 3:40-42.) "The USB cable 42 includes four wires, one pair for sending data to and from the host computer 12, and a second pair for supplying power to the camera 10 from the host computer 12." (Endsley 613 at 3:62-65.)  Endsley 613 (Figure 1) "The system includes a camera 10 connected to a host computer 12 via a USB (universal serial bus) cable 42 connected to a USB digital host interface 14, which also provides power to the camera 10. . . . The camera 10 can acquire both still and motion images. The camera data is

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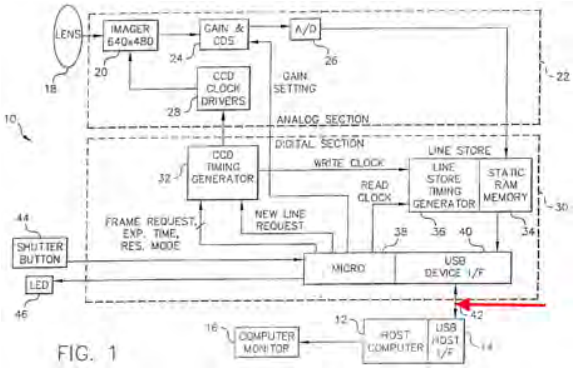
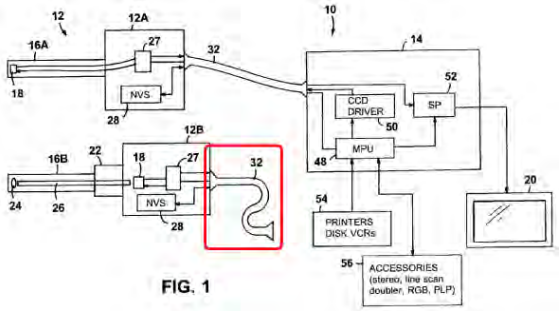
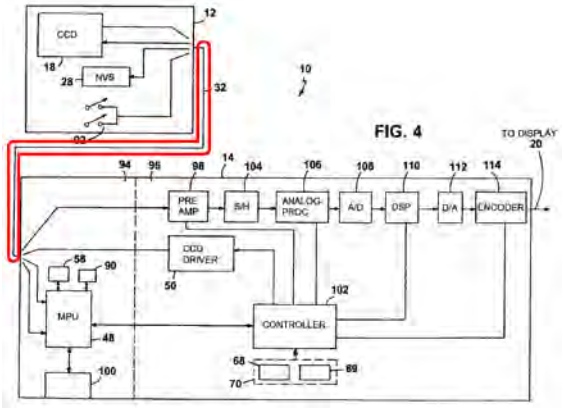
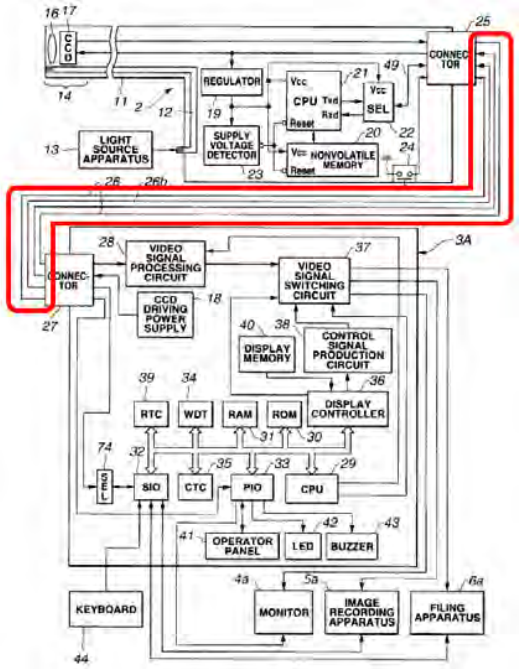
Claims	**Asaida 782**	**in combination with one or more of the following references**
		processed by the host computer 12 to create final images that can be displayed on a computer monitor 16, e.g., transmitted along with audio as part of a 'computer videoconference', etc." (Endsley 471 at 2:50-63.) "The USB cable 42 includes four wires, one pair for sending data to and from the host computer 12, and a second pair to supply power to the camera 10 from the host." (Endsley 471 at 3:46-48.)  FIG. 1 Endsley 471 (Figure 1) "Referring to FIG. 4, in a more detailed view, camera head 12 includes CCD 18 (located, as discussed, either in the head or at the tip of the endoscope), NVS 28 and a set of button switches 92 for system control, and camera processor 14 includes a camera controller 94 and a signal processor 96. Cable 32, which connects camera head 12 to camera processor 14, carries drive signals from CCD driver 50 in

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		signal processor 96, electrical signals from CCD 18 to a preamplifier 98 in signal processor 96, data between NVS 28 and MPU 48 in camera controller 94, and signals from button switches 92 to MPU 48." (Dowdy 082 at 6:48-58.)  FIG. 1 Dowdy 082 (Figure 1)  FIG. 4 Dowdy 082 (Figure 4)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		"The connector 25 of the endoscope 2 is linked to a connector 27 of the image processing apparatus 3A by a cable 26." (Oshima 212 at 7:11-13.)  Oshima 212 (Figure 2) "The CCU 4 also comprises an input connector 30 whereby the CCU may be coupled to camera output connector 14 via a suitable cable 32." (Zu 391 at 3.)

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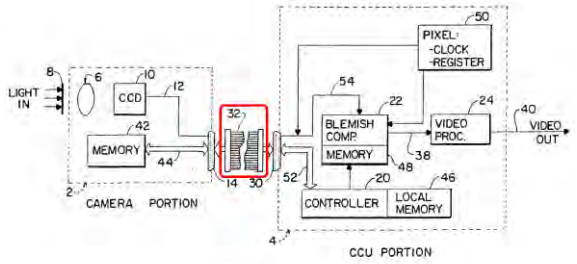
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 FIG. 2 Zu 391 (Figure 2) "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope. The skilled person will appreciate that the wire connection 20 may be an optical connection or may instead use RF or a like means of wireless communication. The miniature endoscopic front-end 10 may be designed for connection to any standard PC input (the USB input for example)." (Adler 940 at 9:24-38.)

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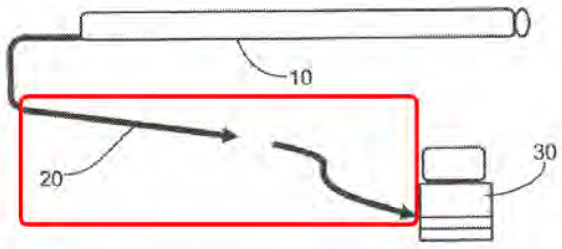
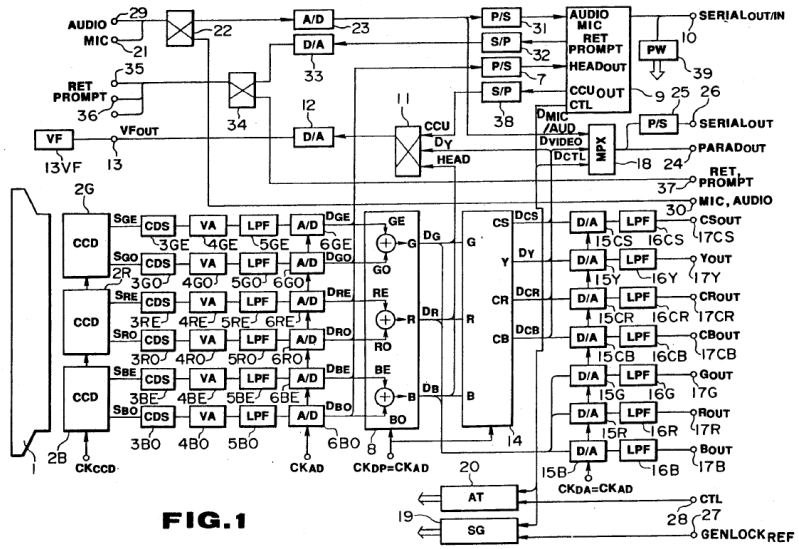
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Adler 940 (Figure 1)
a camera head, connected to said cable and	"FIG. 1 is a block diagram showing an embodiment of a camera head unit of a video camera according to the present invention." (Asaida 782 at 3:44-46.)  FIG.1	"In FIG. 1 and FIG. 2, the circuit configuration of an electronic endoscope according to the embodiment is shown. In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having a number of scanning lines or the like suitable for the scanning line of the NTSC system, and to this CCD 1, a timing generator 16 is connected, and to this timing generator 16, an NTSC crystal oscillator 17, a PAL crystal oscillator 18, and a switching device 19 are provided. Furthermore, a first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU 20, either of the oscillators 17, 18 is selected." (Okada 852 at 4:4-15.)

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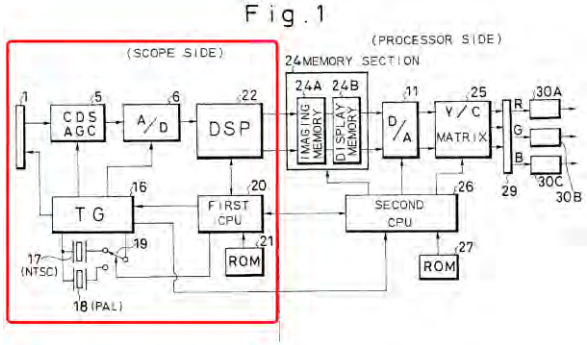
Claims	**Asaida 782**	**in combination with one or more of the following references**
	Asaida 782 (Figure 1) "The encoder/decoder 9 encodes the serial data, that is, the camera output data $HEAD_{OUT}$, supplied from the P/S converter 7, and outputs the encoded data at a serial input/output port 10 over an optical fiber cable, not shown." (Asaida 782 at 5:45-49.) "Thus, with the present video camera unit, the two-line-concurrent three-color imaging output signals S_{RO}, S_{RE}, S_{GO}, S_{GE}, S_{BO} and S_{BE}, obtained by the solid-state image sensors 2R, 2G, and 2B, are changed by the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE into two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}. The two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, are converted by the P/S converter 7 into serial data as the camera output data $HEAD_{OUT}$, which are serially outputted at the serial input/output port 10 by means of the encoder/decoder 9." (Asaida 782 at 5:50-61.)	Fig. 1  Okada 852 (Figure 1) "The camera 10 is connected to a host computer 12 via a USB (universal serial bus) digital host interface 14, which also provides power to the camera 10. . . . The camera 10 can acquire both still and motion images. The camera data is processed by the host computer 12 to create final images that can be displayed on a computer monitor 16, e.g., transmitted along with audio as part of a "computer videoconference", etc." (Endsley 613 at 3:9-21.)

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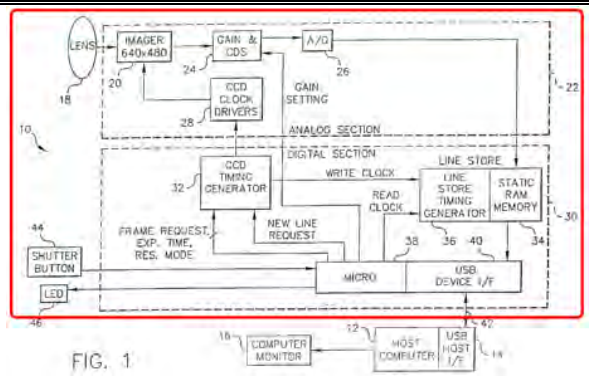
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 FIG. 1 Endsley 613 (Figure 1) "The system includes a camera 10 connected to a host computer 12 via a USB (universal serial bus) cable 42 connected to a USB digital host interface 14, which also provides power to the camera 10. . . . The camera 10 can acquire both still and motion images. The camera data is processed by the host computer 12 to create final images that can be displayed on a computer monitor 16, e.g., transmitted along with audio as part of a 'computer videoconference', etc." (Endsley 471 at 2:50-63.)

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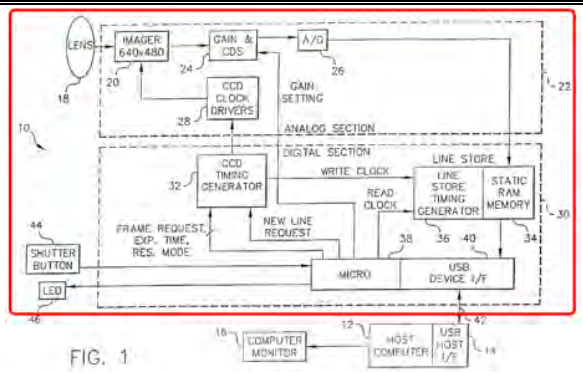
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 FIG. 1 Endsley 471 (Figure 1) "Referring to FIG. 1, a video endoscopy or borescope system 10 includes a camera head 12 and a camera processor 14. Camera head 12 includes an endoscope 16 for insertion into a region such as a body cavity, and an imaging device, such as a CCD 18, that produces electrical signals representative of an optical image at the distal end of endoscope 16. Camera processor 14 processes the electrical signals produced by camera head 12 to generate a video image that is displayed on a video monitor 20." (Dowdy 082 at 3:24-32.) "By varying parameters such as the type of endoscope, the endoscope mount, and the CCD optical format size, camera head 12 can be configured in numerous ways, all of which can produce different electrical signals to represent the same optical image. As illustrated in FIG. 1, camera head 12A includes an electronic endoscope 16A, while camera head

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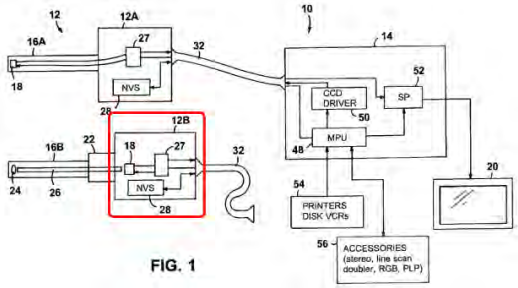
Claims	**Asaida 782**	**in combination with one or more of the following references**
		12B includes an optical endoscope 16B. Electronic endoscope 16A is integrally connected to camera head 12A and has a CCD 18 positioned behind focussing optics (not shown) at its distal end. By contrast, optical endoscope 16B has a mount 22 for attachment to camera head 12B, and includes an optical lens 24 positioned at its distal tip and an optical fiber 26 or relay lens assembly that transmits an image from optical lens 24 to a CCD 18 positioned, with support circuitry 27, within camera head 16B." (Dowdy 082 at 3:33-47 (emphasis added).)  FIG. 1 Dowdy 082 (Figure 1) "Referring to FIG. 4, in a more detailed view, camera head 12 includes CCD 18 (located, as discussed, either in the head or at the tip of the endoscope), NVS 28 and a set of button switches 92 for system control, and camera processor 14 includes a camera controller 94 and a signal processor 96. Cable 32, which connects camera head 12 to camera processor 14, carries drive signals from CCD driver 50 in

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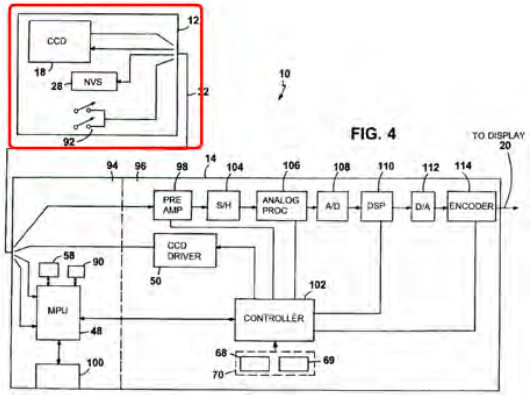
Claims	**Asaida 782**	**in combination with one or more of the following references**
		signal processor 96, electrical signals from CCD 18 to a preamplifier 98 in signal processor 96, data between NVS 28 and MPU 48 in camera controller 94, and signals from button switches 92 to MPU 48." (Dowdy 082 at 6:48-58 (emphasis added).)  Dowdy 082 (Figure 4) "An endoscope system 1 in accordance with the first embodiment of the present invention shown in FIG. 1 consists broadly of an endoscope 2, and connected apparatuses (or peripheral equipment) to be selectively connected to the endoscope. The connected apparatuses include an image processing apparatus 3A, an image processing apparatus 3B, a cleaning apparatus 3C, a filing apparatus 3D, a monitor 4 a, an image recording apparatus 5 a, a filing apparatus 6 a, a monitor 4 b, an image recording apparatus 5 b, a filing apparatus 6 b, a filing apparatus 6 c,

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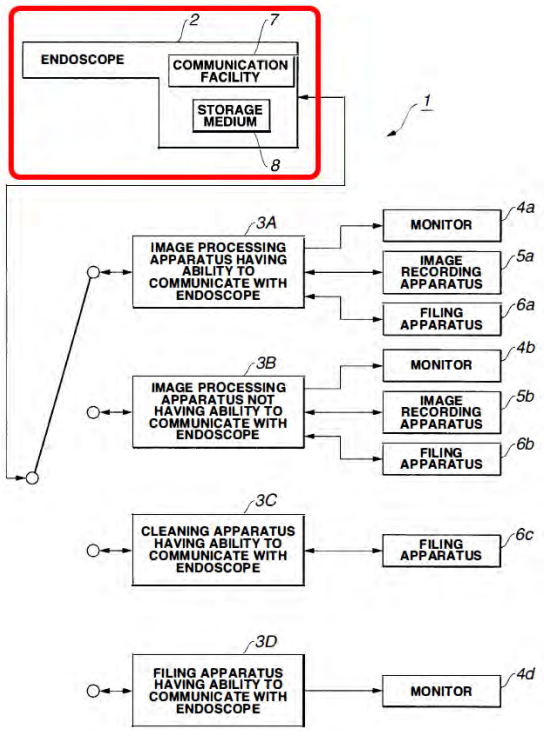
Claims	**Asaida 782**	**in combination with one or more of the following references**
		and a monitor 4 d. The image processing apparatus 3A has the ability to communicate with the endoscope 2. . . ." (Oshima 212 at 5:15-26.)  Oshima 212 (Figure 1) "FIG. 2 is a block diagram showing in detail the endoscope 2 and the image processing apparatus 3A having the communicating ability which are employed in the present

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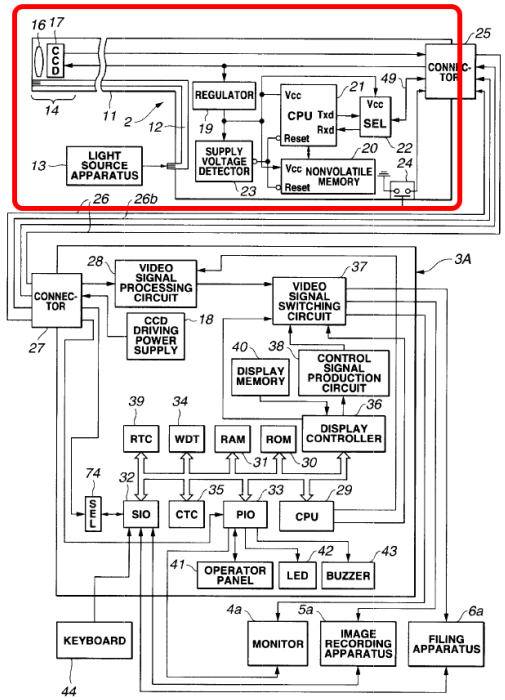
Claims	**Asaida 782**	**in combination with one or more of the following references**
		embodiment." (Oshima 212 at 6:34-37.)  Oshima 212 (Figure 2) "The connector 25 of the endoscope 2 is linked to a connector 27 of the image processing apparatus 3A by a cable 26." (Oshima 212 at 7:11-13.) "Figure 1 illustrates a prior art video system comprising a camera 2 and a CCU 4. The camera comprises an optical

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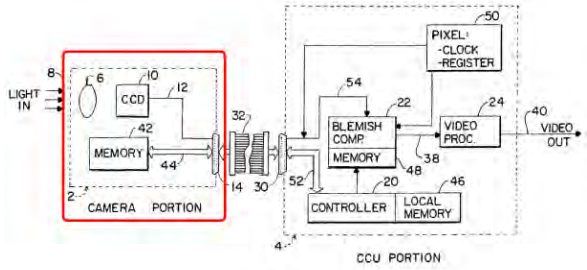
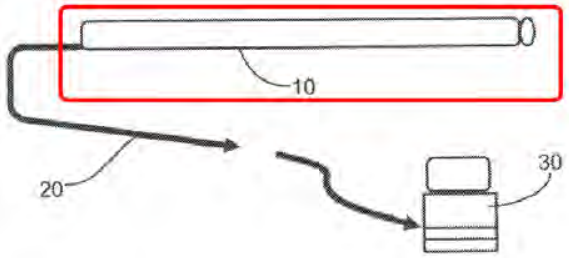
Claims	**Asaida 782**	**in combination with one or more of the following references**
		system 6 and a CCD array 10. The latter produces a video signal output when it is illuminated with light via optical system 6. This video signal output is fed by an internal transmission bus 12 to an output connector 14 which forms part of the camera." (Zu 391 at 3.)  FIG. 2 Zu 391 (Figure 2) "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope. The skilled person will appreciate that the wire connection 20 may be an optical connection or may instead use RF or a like means of wireless

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		communication. The miniature endoscopic front-end 10 may be designed for connection to any standard PC input (the USB input for example)." (Adler 940 at 9:24-38.)  Adler 940 (Figure 1)
an endoscope, for providing the stream of digital video data, said camera head including;	Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005) (citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)). Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	"In FIG. 1 and FIG. 2, the circuit configuration of an electronic endoscope according to the embodiment is shown. In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having a number of scanning lines or the like suitable for the scanning line of the NTSC system, and to this CCD 1, a timing generator 16 is connected, and to this timing generator 16, an NTSC crystal oscillator 17, a PAL crystal oscillator 18, and a switching device 19 are provided. Furthermore, a first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU 20, either of the oscillators 17, 18 is selected." (Okada 852 at 4:4-15.)

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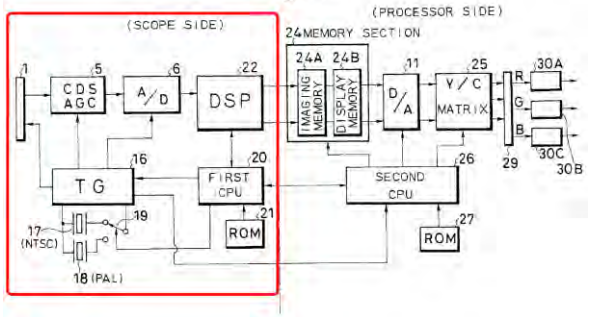
Claims	**Asaida 782**	**in combination with one or more of the following references**
		Fig. 1  Okada 852 (Figure 1) "Referring to FIG. 1, a video endoscopy or borescope system 10 includes a camera head 12 and a camera processor 14. Camera head 12 includes an endoscope 16 for insertion into a region such as a body cavity, and an imaging device, such as a CCD 18, that produces electrical signals representative of an optical image at the distal end of endoscope 16. Camera processor 14 processes the electrical signals produced by camera head 12 to generate a video image that is displayed on a video monitor 20." (Dowdy 082 at 3:24-32.) "By varying parameters such as the type of endoscope, the endoscope mount, and the CCD optical format size, camera head 12 can be configured in numerous ways, all of which can produce different electrical signals to represent the same optical image. As illustrated in FIG. 1, camera head 12A includes an electronic endoscope 16A, while camera head

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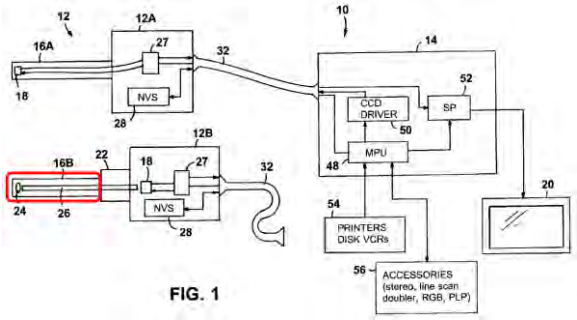
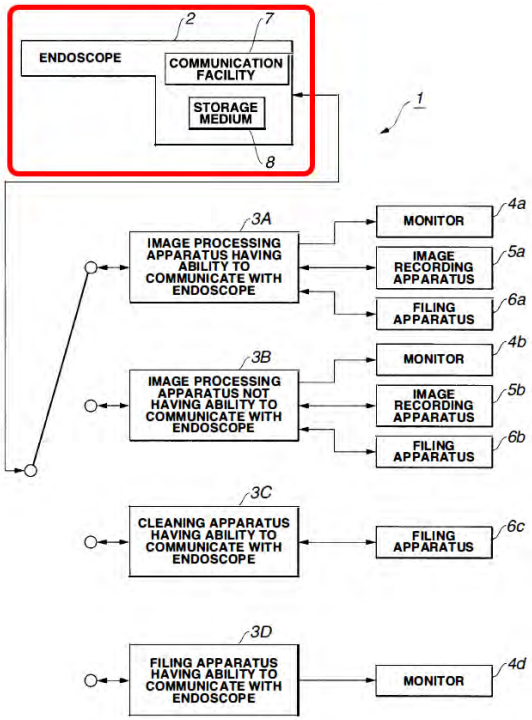
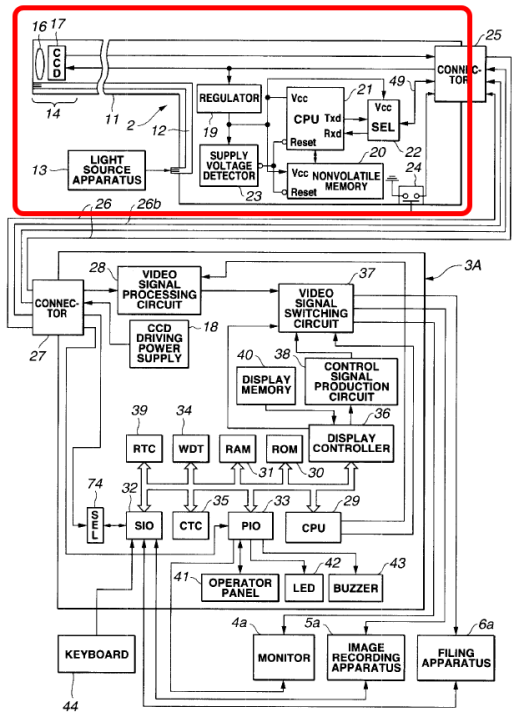
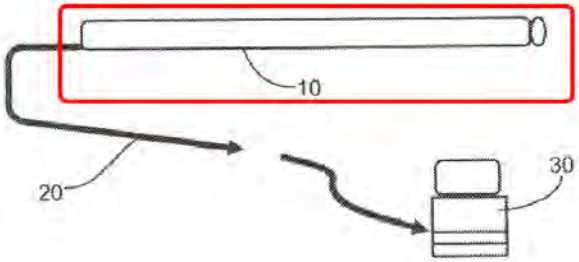
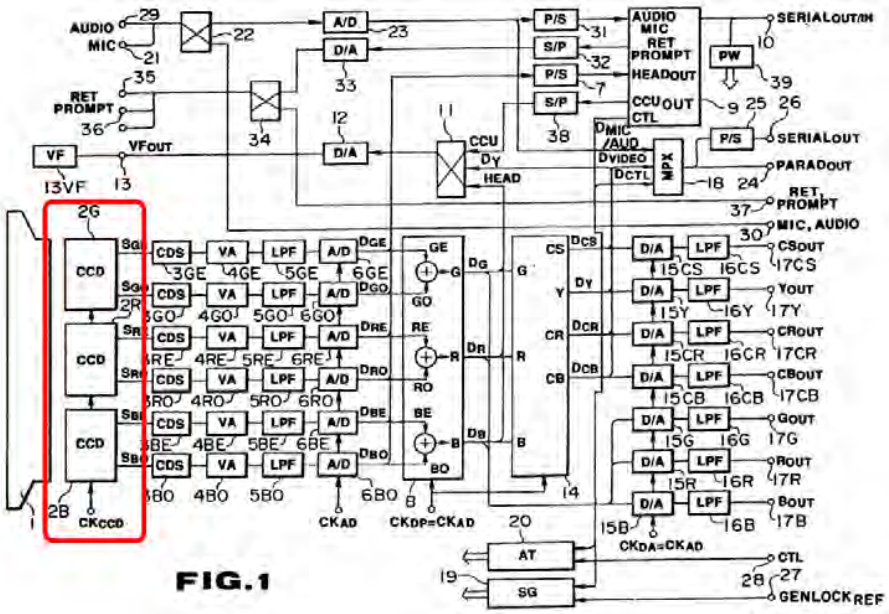
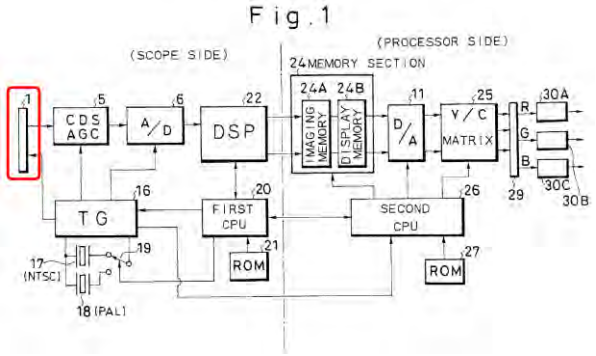
Claims	**Asaida 782**	**in combination with one or more of the following references**
		12B includes an optical endoscope 16B. Electronic endoscope 16A is integrally connected to camera head 12A and has a CCD 18 positioned behind focussing optics (not shown) at its distal end. By contrast, optical endoscope 16B has a mount 22 for attachment to camera head 12B, and includes an optical lens 24 positioned at its distal tip and an optical fiber 26 or relay lens assembly that transmits an image from optical lens 24 to a CCD 18 positioned, with support circuitry 27, within camera head 16B." (Dowdy 082 at 3:33-47 (emphasis added).)  FIG. 1 Dowdy 082 (Figure 1) "An endoscope system 1 in accordance with the first embodiment of the present invention shown in FIG. 1 consists broadly of an endoscope 2, and connected apparatuses (or peripheral equipment) to be selectively connected to the endoscope. The connected apparatuses include an image processing apparatus 3A, an image processing apparatus 3B, a cleaning apparatus 3C, a filing

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		apparatus 3D, a monitor 4 a, an image recording apparatus 5 a, a filing apparatus 6 a, a monitor 4 b, an image recording apparatus 5 b, a filing apparatus 6 b, a filing apparatus 6 c, and a monitor 4 d. The image processing apparatus 3A has the ability to communicate with the endoscope 2. . . ." (Oshima 212 at 5:15-26.)  Oshima 212 (Figure 1)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		"FIG. 2 is a block diagram showing in detail the endoscope 2 and the image processing apparatus 3A having the communicating ability which are employed in the present embodiment." (Oshima 212 at 6:34-37.)  Oshima 212 (Figure 2) "The connector 25 of the endoscope 2 is linked to a connector 27 of the image processing apparatus 3A by a

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		cable 26." (Oshima 212 at 7:11-13.) "This invention relates to compensating for CCD blemishes in video cameras and more particularly to cameras that are designed to be used interchangeably with camera control units, notably but not exclusively video cameras that are incorporated in endoscopes for use with medical imaging systems." (Zu 391 at 1.) "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope. The skilled person will appreciate that the wire connection 20 may be an optical connection or may instead use RF or a like means of wireless communication. The miniature endoscopic front-end 10 may be designed for connection to any standard PC input (the USB input for example)." (Adler 940 at 9:24-38.)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Adler 940 (Figure 1)
an imager,	"In the camera head unit, shown in FIG. 1, the present invention includes a three CCD solid state color imaging device in which the imaging light from an object in a field of view is separated by an imaging pickup device 1 into three primary color components and in which three primary color object images are produced by three solid state imaging sensors 2R, 2G and 2B." (Asaida 782 at 4:9-15.)	"In FIG. 1 and FIG. 2, the circuit configuration of an electronic endoscope according to the embodiment is shown. In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having a number of scanning lines or the like suitable for the scanning line of the NTSC system, and to this CCD 1, a timing generator 16 is connected, and to this timing generator 16, an NTSC crystal oscillator 17, a PAL crystal oscillator 18, and a switching device 19 are provided. Furthermore, a first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU 20, either of the oscillators 17, 18 is selected." (Okada 852 at 4:4-15.)

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
	 FIG.1 Asaida 782 (Figure 1)	 Okada 852 (Figure 1) "The camera 10 includes an optical section 18 for imaging light from a subject upon an electronic image sensor 20. A preferred image sensor is a Kodak KAI-0320CM interline transfer, progressive-scan charge-coupled-device (CCD) image sensor with a usable active image area having 640 columns and 480 rows of color photoelements arranged in the well-known Bayer color filter array pattern (see U.S. Pat. No. 3,971,065 for a description of the Bayer pattern)." (Endsley 613 at 3:24-31.)

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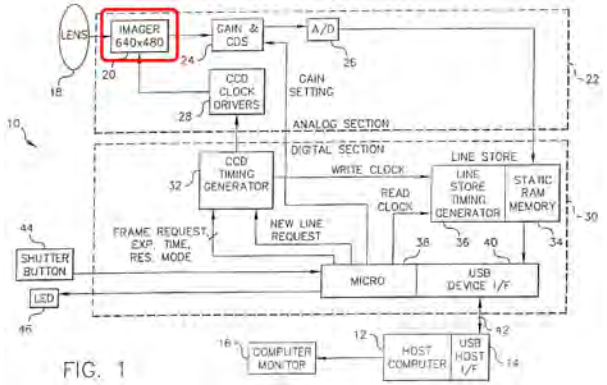
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 FIG. 1 Endsley 613 (Figure 1) "The camera 10 includes an optical section 18 from imaging light from a subject upon an electronic image sensor 20. A preferred image sensor is a Kodak KAI-0320CM interline transfer, progressive-scan charge-coupled-device (CCD) image sensor with a usable active image area having 640 columns and 480 rows of color photoelements arranged in the well-known Bayer color filter array patters shown in FIG. 2 (see U.S. Pat. No. 3,971,065 for further description of the Bayer pattern). As shown in FIG. 2, the sensor 20 includes light shielded vertical registers 50 and a horizontal readout register 52. Details of a single photoelement 54 are shown in FIG. 3. Each photoelement 54 includes a light-sensitive photodiode 56 supported on a substrate 58 adjacent the light-shielded vertical register 50." (Endsley 471 at 2:66-3:12.)

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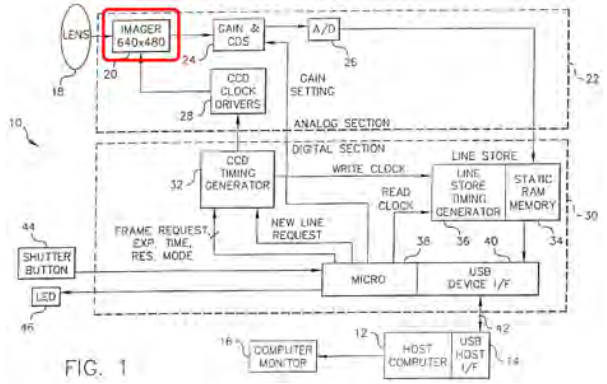
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 FIG. 1 Endsley 471 (Figure 1) "Referring to FIG. 1, a video endoscopy or borescope system 10 includes a camera head 12 and a camera processor 14. Camera head 12 includes an endoscope 16 for insertion into a region such as a body cavity, and an imaging device, such as a CCD 18, that produces electrical signals representative of an optical image at the distal end of endoscope 16. Camera processor 14 processes the electrical signals produced by camera head 12 to generate a video image that is displayed on a video monitor 20." (Dowdy 082 at 3:24-32.) "By varying parameters such as the type of endoscope, the endoscope mount, and the CCD optical format size, camera head 12 can be configured in numerous ways, all of which can produce different electrical signals to represent the same optical image. As illustrated in FIG. 1, camera head 12A

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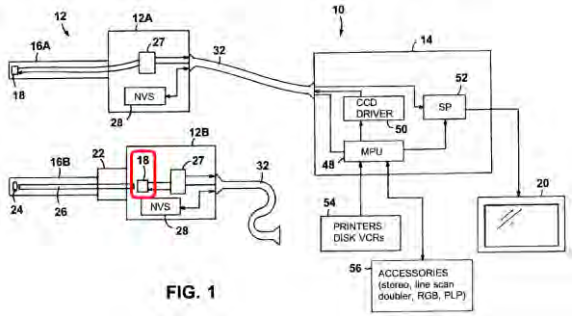
Claims	**Asaida 782**	**in combination with one or more of the following references**
		includes an electronic endoscope 16A, while camera head 12B includes an optical endoscope 16B. Electronic endoscope 16A is integrally connected to camera head 12A and has a CCD 18 positioned behind focussing optics (not shown) at its distal end. By contrast, optical endoscope 16B has a mount 22 for attachment to camera head 12B, and includes an optical lens 24 positioned at its distal tip and an optical fiber 26 or relay lens assembly that transmits an image from optical lens 24 to a CCD 18 positioned, with support circuitry 27, within camera head 16B." (Dowdy 082 at 3:33-47 (emphasis added).)  FIG. 1 Dowdy 082 (Figure 1) "The output of preamplifier 98 is connected to the input of a sample and hold circuit 104 that passes only portions of the output. The output of sample and hold circuit 104 is supplied to an analog processing circuit 106 that is also controlled by signal processing controller 102. In controlling analog processing circuit 106, signal processing controller 102 uses

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		values from lookup table 68 that have been loaded into memory 70. As discussed above, if these values have been modified or replaced by MPU 48 based on information from NVS 28 of camera head 12, then analog processing circuit 106 will be affected by the new values." (Dowdy 082 at 7:27-37.) "An analog to digital converter 108 converts the output of analog processing circuit 106 into a digital signal, and supplies the digital signal to a digital signal processor (DSP) 110 that is controlled by signal processing controller 102. Once again, signal processing controller 102 controls digital signal processor using values from memory 70 that can be modified or replaced by MPU 48 in response to information from NVS 28 of camera head 12." (Dowdy 082 at 7:38-45.) Because digital-to-analog conversion takes place in the CCU, the imager 18 must generate an analog stream of video data. "The illuminated object is imaged by a solid-state imaging device located on an image plane, for example, a charge-coupled device (CCD) 17 through an objective 16 locked in an observation window formed in the distal part 14. The CCD 17 photoelectrically converts the optical image." (Oshima 212 at 6:49-53.)

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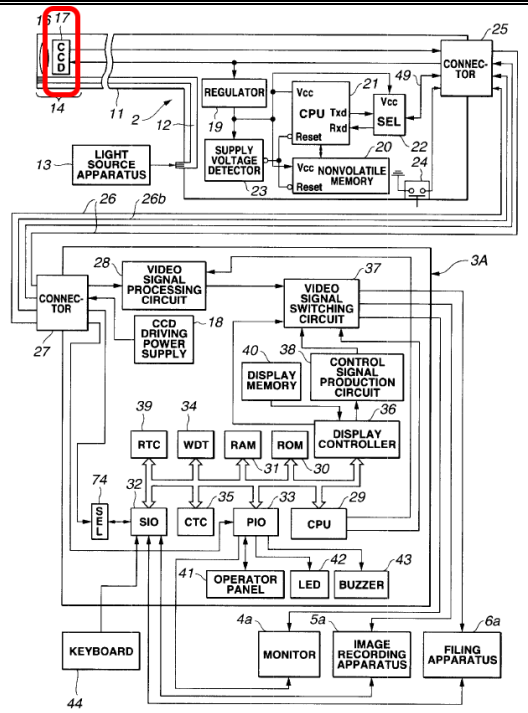
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Oshima 212 (Figure 2) "Figure 1 illustrates a prior art video system comprising a camera 2 and a CCU 4. The camera comprises an optical system 6 and a CCD array 10. The latter produces a video signal output when it is illuminated with light via optical system 6. This video signal output is fed by an internal transmission bus 12 to an output connector 14 which forms part of the camera." (Zu 391 at 3 (emphasis added).)

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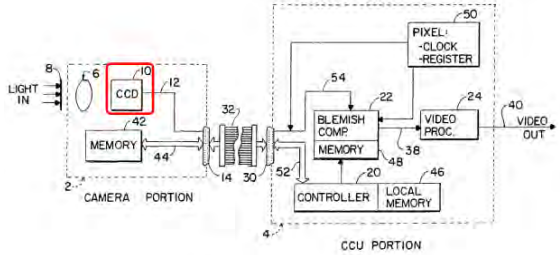
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 FIG. 2 Zu 391 (Figure 2) "Reference is now made to FIG. 2, which is an internal block diagram of an endoscope according to a preferred embodiment of the present invention. A miniature endoscope 40 is connected by a wire 42 to an adapter 44. The endoscope 40 comprises an image sensor 46 which may typically comprise a CMOS or CCD or like sensing technology, an optical assembly 48, a light or illumination source 50, communication interface 52 and controller 54. The wired unit of FIG. 2 preferably includes a voltage regulator 56." (Adler 940 at 9:48-57.)

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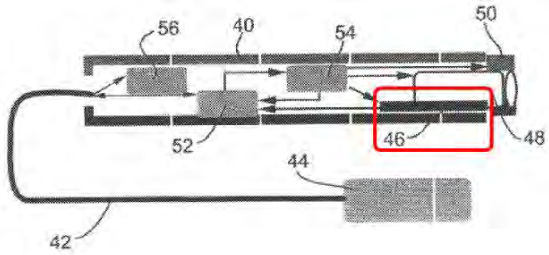
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Adler 940 (Figure 2) "The present invention relates generally to the field of interface circuits, and more particularly, to interface circuitry for providing selectable single-ended and differential signal output from a CMOS image sensor to an external digital signal processor." (Chung 290 at 1:11-15.) "One of the advantages of CMOS image sensors (CMOS imagers) over CCD imagers is that the CMOS imager chip can include digital signal processing circuitry. In practice, the signal processing is more often performed on a companion chip, in order to provide greater application flexibility. However, CMOS imagers often have integrated analog to digital converters to convert the analog signal to a digital bit stream that can be processed by the companion chip. The digitized information then must be transferred to companion chip or other external devices for picture storage, processing, or transmission." (Chung 290 at 1:17-27.) "FIG. 4 illustrates CMOS video imaging sensing circuitry

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		according to the preferred embodiment disclosed in co-pending U.S. application Ser. No 09/062,343. This circuitry includes a CMOS image sensor chip 50 and an image processor chip 52. The CMOS image sensor chip 50 typically includes a number of light responsive CMOS pixel sensors which develop analog signals representative of an image. These analog signals are then A to D converted by the ADC circuit to form digital signals Din0, Din1 . . . Dinn. The image processor chip 52 includes a data processor 53 which performs various manipulations of the image data such as compression and color processing. The processor 53 may be software driven or a hardware embodiment." (Chung 290 at 2:14-26.)

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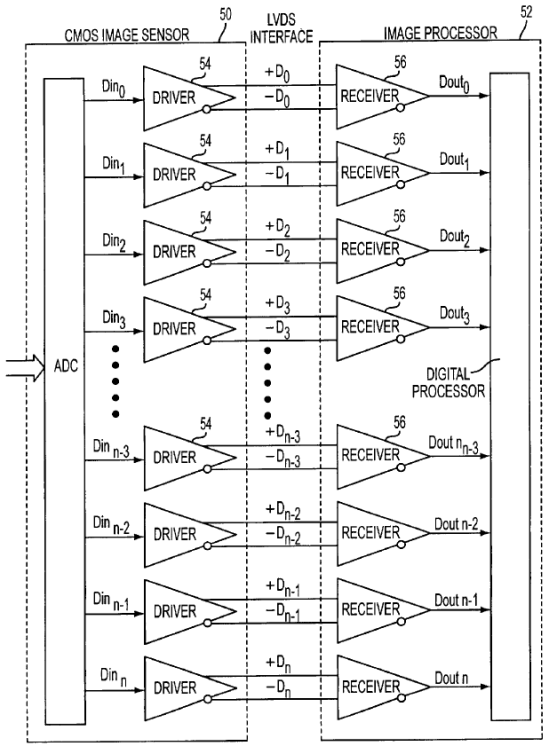
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Chung 290 (Figure 4)
including an analog to digital converter for generating	"The two-line-concurrent three-color imaging output signals S_{RO}, S_{RE}, S_{GO}, S_{GE}, S_{BO} and S_{BE}, processed for level adjustment by the level adjustment circuits 4RO, 4RE, 4GO, 4GE, 4BO and 4BE, are transmitted by means of low-pass filters 5RO, 5RE, 5GO, 5GE, 5BO and 5BE, respectively, to A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, functioning as analog/ digital converting means,	"[T]o the CCD 1, an AGC (automatic gain control) circuit including a CDS (correlative double sampling) circuit is connected similarly to that in the prior art, and to this AGC circuit 5, a DSP (digital signal processor) circuit 22 is connected through an A/D converter 6." (Okada 852 at 4:29-33.)

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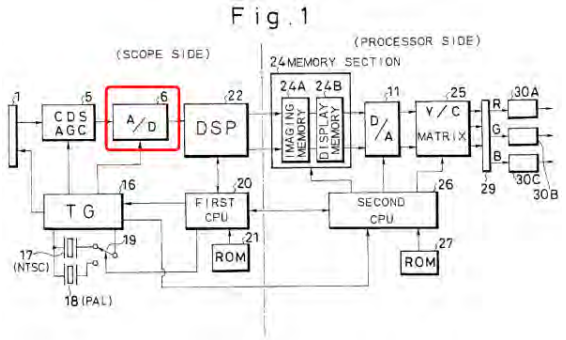
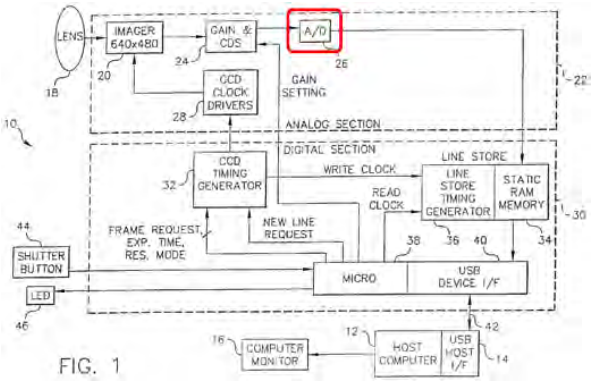
Claims	**Asaida 782**	**in combination with one or more of the following references**
the stream of digital video data;	respectively." (Asaida 782 at 5:14-22.) "A driving clock CK_{AD} having a frequency four times the frequency of the color subcarrier frequency f_{SC}, or $4f_{SC}$, is supplied to the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, by means of a timing generator, not shown. The A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE digitize the two-line-concurrent three-color imaging output signals S_{RO}, S_{RE}, S_{GO}, S_{GE}, S_{BO} and S_{BE} with the $4f_{sc}$ driving clock CK_{AD} to produce two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, respectively. The two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, produced by the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, are supplied to a parallel/serial converter (P/S converter) 7 and to a signal processing section 8." (Asaida 782 at 5:23-37.)	 Okada 852 (Figure 1) "An analog section 22 in the camera 10 includes the sensor 20, a CDS/gain block 24 for performing correlated double sampling (CDS) and setting the analog gain, an analog-to-digital (A/D) converter 26 for converting the analog output signal from the CCD sensor 20 to, e.g., an 8-bit digital signal, and CCD clock drivers 28 for clocking the sensor 20." (Endsley 613 at 3:31-37.)  FIG. 1

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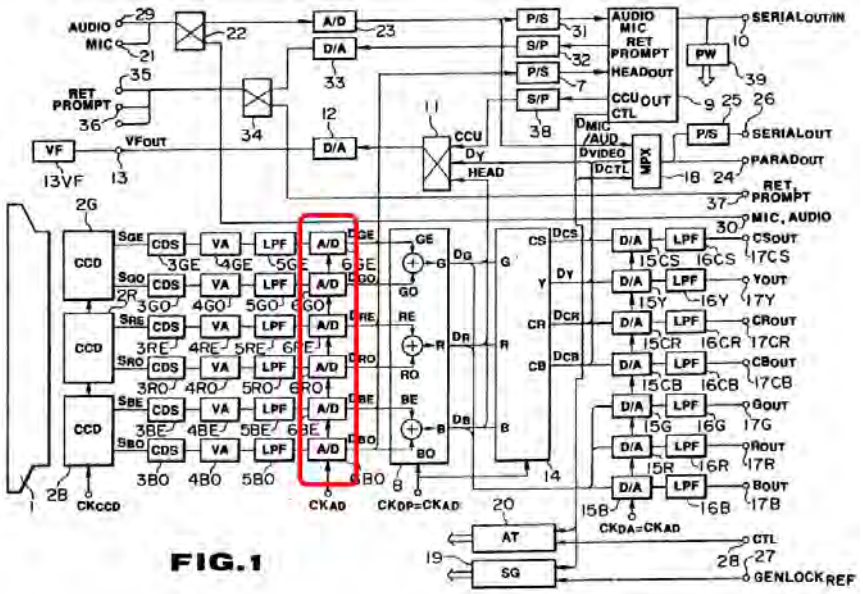
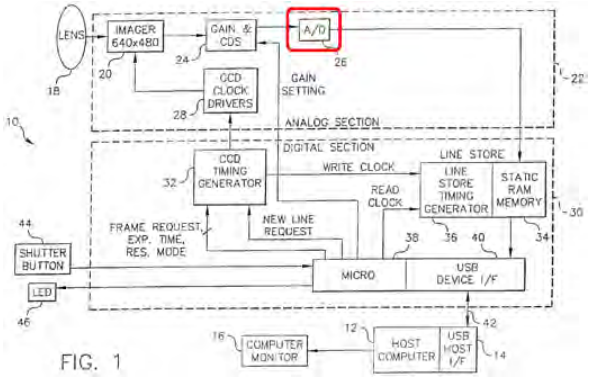
Claims	**Asaida 782**	**in combination with one or more of the following references**
	 FIG.1 Asaida 782 (Figure 1)	Endsley 613 (Figure 1) "An analog section 22 in the camera 10 includes the sensor 20, a CDS/gain block 24 for performing correlated double sampling (CDS) and setting the analog gain, an analog-to-digital (A/D) converter 26 for converting the analog output signal from the CCD sensor 20 to, e.g., an 8-bit digital signal, and CCD clock drivers 28 for clocking the sensor 20." (Endsley 471 at 3:13-18.)  FIG. 1 Endsley 471 (Figure 1) "Reference is now made to FIG. 4, which is an schematic block diagram of the miniature endoscope according to a preferred embodiment of the present invention. Parts that are identical to those shown above are given the same reference numerals and are not referred to again except as necessary

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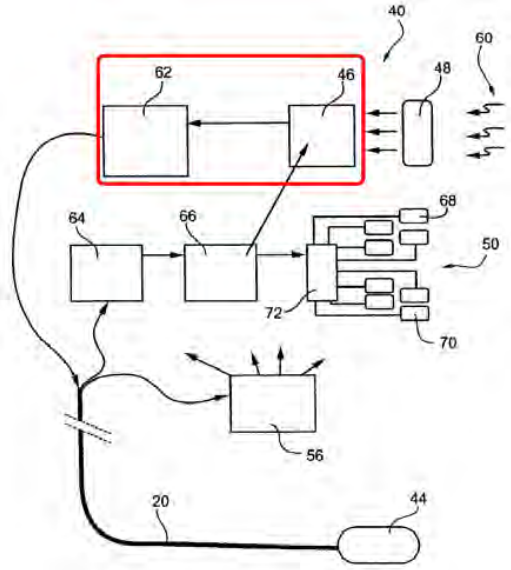
Claims	**Asaida 782**	**in combination with one or more of the following references**
		for an understanding of the present embodiment. Optical assembly 48 receives light, indicated by arrows 60, from an object being viewed. The light is processed by optical assembly 48, as will be explained below, to reach image sensor 46 were it is converted from photons into electrical signals. The electrical signals are digitized and passed to a transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Adler 940 at 10:7-19 (emphasis added).)  Adler 940 (Figure 4) Because "the electrical signals are digitized and passed to a

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		transmitting device 62" in the camera head, the camera head must contain a converter for converting an analog stream of video data into a stream of digital video data. "One of the advantages of CMOS image sensors (CMOS imagers) over CCD imagers is that the CMOS imager chip can include digital signal processing circuitry. In practice, the signal processing is more often performed on a companion chip, in order to provide greater application flexibility. However, CMOS imagers often have integrated analog to digital converters to convert the analog signal to a digital bit stream that can be processed by the companion chip. The digitized information then must be transferred to companion chip or other external devices for picture storage, processing, or transmission." (Chung 290 at 1:17-27 (emphasis added).) "FIG. 4 illustrates CMOS video imaging sensing circuitry according to the preferred embodiment disclosed in co-pending U.S. application Ser. No 09/062,343. This circuitry includes a CMOS image sensor chip 50 and an image processor chip 52. The CMOS image sensor chip 50 typically includes a number of light responsive CMOS pixel sensors which develop analog signals representative of an image. These analog signals are then A to D converted by the ADC circuit to form digital signals Din0, Din1 . . . Dinn. The image processor chip 52 includes a data processor 53 which performs various manipulations of the image data such as compression and color processing. The processor 53 may be software driven or a hardware embodiment." (Chung 290 at

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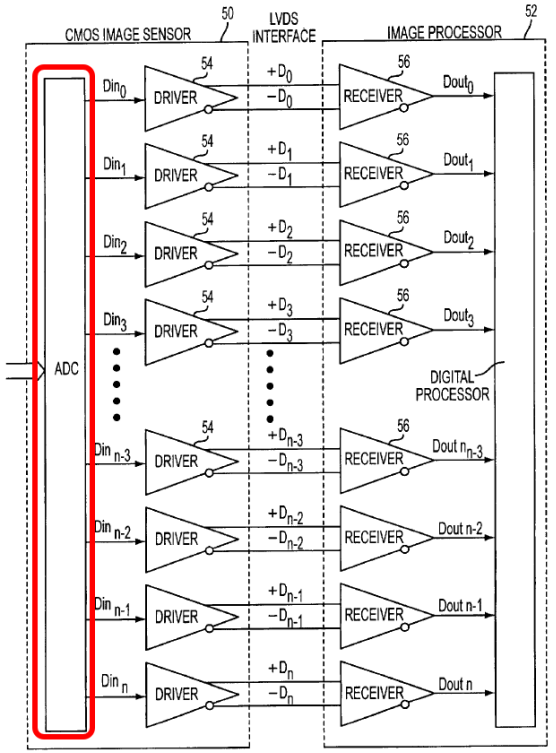
Claims	**Asaida 782**	**in combination with one or more of the following references**
		2:14-26.)  Chung 290 (Figure 4)
a serializer, for serializing the stream	"A driving clock CK_{AD} having a frequency four times the frequency of the color subcarrier frequency f_{SC}, or $4f_{SC}$, is supplied to the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, by means of a timing generator, not shown. The A/D converters 6RO, 6RE, 6GO,	To the extent this element is not expressly disclosed, it is inherent in Endsley 613 by virtue of disclosing and claiming USB as a communications medium.

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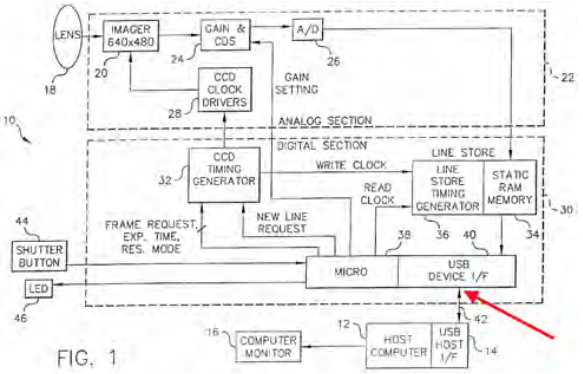
Claims	**Asaida 782**	**in combination with one or more of the following references**
of digital video data for continuous transmission over said cable	6GE, 6BO and 6BE digitize the two-line-concurrent three-color imaging output signals S_{RO}, S_{RE}, S_{GO}, S_{GE}, S_{BO} and S_{BE} with the $4f_{sc}$ driving clock CK_{AD} to produce two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, respectively. The two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, produced by the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, are supplied to a parallel/serial converter (P/S converter) 7 and to a signal processing section 8." (Asaida 782 at 5:23-37.) "The P/S converter 7 changes the two-line-concurrent digital three color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, supplied from the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO, and 6BE, from parallel data into serial data. The serial data, produced by the P/S converter 7, are supplied as camera output data $HEAD_{OUT}$ to a light-transmitting encoder/decoder 9." (Asaida 782 at 5:38-44.) "The encoder/decoder 9 encodes the serial data, that is, the camera output data $HEAD_{OUT}$, supplied from the P/S converter 7, and outputs the encoded data at a serial input/output port 10 over an optical fiber cable, not shown." (Asaida 782 at 5:45-49.)	Specifically, section 10.2.2 of the USB Specification Revision 1.0 (Jan. 15, 1996) explains that "[t]he actual transmission of data across the physical USB takes place as a serial bit stream. A Serial Interface Engine (SIE), whether implemented as part of the host or a USB device, handles the serialization and deserialization of USB transmissions. On the host, this SIE is part of the host controller." (USB Spec. Rev. 1.0 at 200.) Thus, in order for USB to be implemented as disclosed and claimed in Endsley 613, there must be "a serializer, for serializing the stream of digital video data for transmission over said cable."  Endsley 613 (Figure 1) To the extent this element is not expressly disclosed, it is inherent in Endsley 471 by virtue of disclosing and claiming USB as a communications medium.

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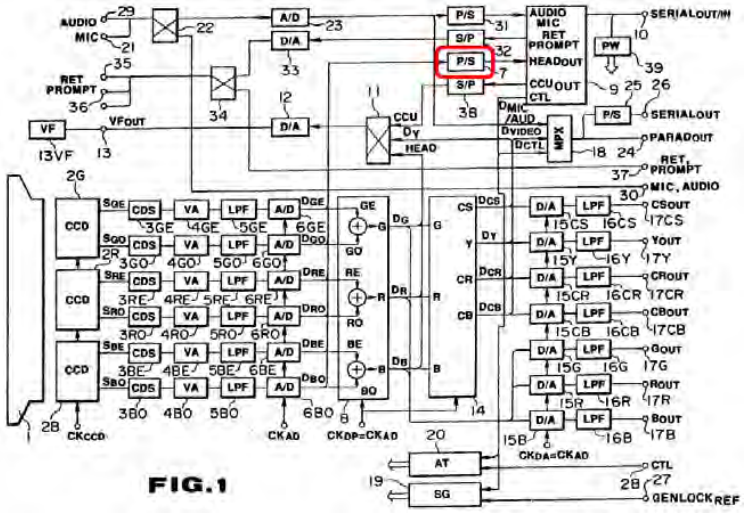
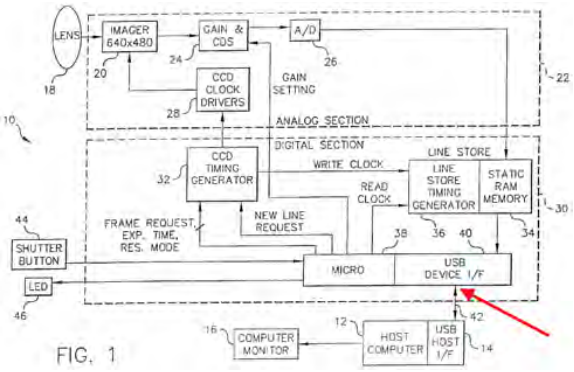
Claims	**Asaida 782**	**in combination with one or more of the following references**
	 FIG.1	Specifically, section 10.2.2 of the USB Specification Revision 1.0 (Jan. 15, 1996) explains that "[t]he actual transmission of data across the physical USB takes place as a serial bit stream. A Serial Interface Engine (SIE), whether implemented as part of the host or a USB device, handles the serialization and deserialization of USB transmissions. On the host, this SIE is part of the host controller." (USB Spec. Rev. 1.0 at 200.) Thus, in order for USB to be implemented as disclosed and claimed in Endsley 471, there must be "a serializer, for serializing the stream of digital video data for transmission over said cable."  FIG. 1 Endsley 471 (Figure 1) "Reference is now made to FIG. 1, which is a basic block diagram of a basic configuration of an endoscope according

U.S. PATENT NO. 7,471,310		
Claims	**Asaida 782**	**in combination with one or more of the following references**
		to a first embodiment of the present invention. The figure shows a basic configuration of the endoscopic system including interconnections. The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope. The skilled person will appreciate that the wire connection 20 may be an optical connection or may instead use RF or a like means of wireless communication. The miniature endoscopic front-end 10 may be designed for connection to any standard PC input (the USB input for example)." (Adler 940 at 9:24-38 (emphasis added).) "Reference is now made to FIG. 4, which is an schematic block diagram of the miniature endoscope according to a preferred embodiment of the present invention. Parts that are identical to those shown above are given the same reference numerals and are not referred to again except as necessary for an understanding of the present embodiment. Optical assembly 48 receives light, indicated by arrows 60, from an object being viewed. The light is processed by optical assembly 48, as will be explained below, to reach image sensor 46 were it is converted from photons into electrical signals. The electrical signals are digitized and passed to a transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Adler 940 at 10:7-19 (emphasis added).)

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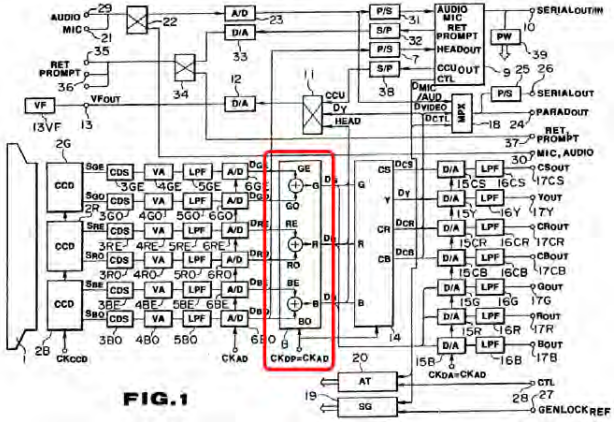
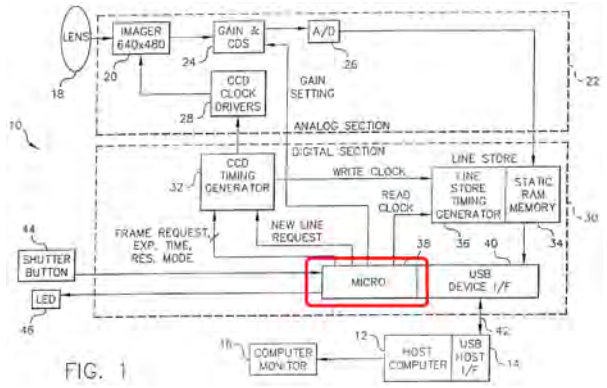
Claims	**Asaida 782**	**in combination with one or more of the following references**
		Because both USB and LVDS are contemplated by Adler 940 as a means for transmitting the stream of digital video data over cable 20, both of which are serial communication protocols, the camera head must include a component that a serializes the digital video data.
a processor; and	"The signal processing section 8 adds the two-line-concurrent digital three-color signals D_{RO}, D_{RE}, D_{GO}, D_{GE}, D_{BO} and D_{BE}, supplied from the A/D converters 6RO, 6RE, 6GO, 6GE, 6BO and 6BE, for each of the color signals, in such a manner that switching between upper and lower lines on both sides of a center line is done on a field-by-field basis to form interlaced digital three-color signals D_R, D_G and D_B. The signal processing section 8 also processes the digital three color signals D_R, D_G and D_B using, for example, gamma correction and image enhancement." (Asaida 782 at 5:62-6:4.)  FIG.1	"A digital section 30 includes a CCD timing generator 32, a static RAM memory 34, a line store timing generator 36, a microprocessor 38, and a USB device interface 40." (Endsley 613 at 3:38-40.) "The microprocessor 38, which may be the Intel 82930 microprocessor, reads data from the line store 34, and transfers the data t the computer 12 via the USB interface 40 (which may be incorporated as part of the microprocessor 38)." (Endsley 613 at 3:58-62.)  FIG. 1

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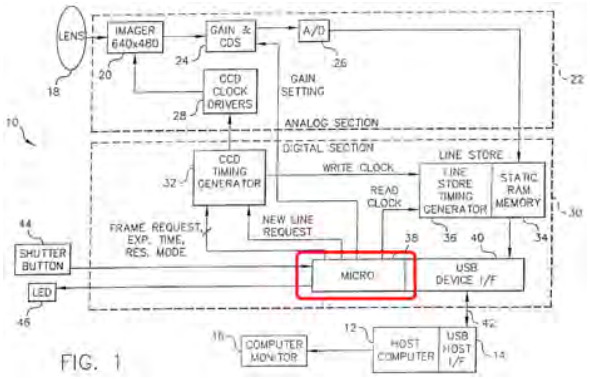
Claims	**Asaida 782**	**in combination with one or more of the following references**
	Asaida 782 (Figure 1) Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005) (citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)). Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	Endsley 613 (Figure 1) "A digital section 30 includes a CCD timing generator 32, a static RAM line store memory 34, a line store timing generator 36, a microprocessor 38, and a USB device interface 40." (Endsley 471 at 3:19-22.) "The USB interface 40, which may be incorporated as part of the microprocessor 38, such as the Intel 82930 microprocessor, reads data from the line store 34." (Endsley 471 at 3:43-46.)  FIG. 1 Endsley 471 (Figure 1) "As shown in FIG. 1, camera processor 14 includes a microprocessing unit ("MPU") 48, a CCD driver 50, and signal processing ("SP") circuitry 52. In operation, MPU 48

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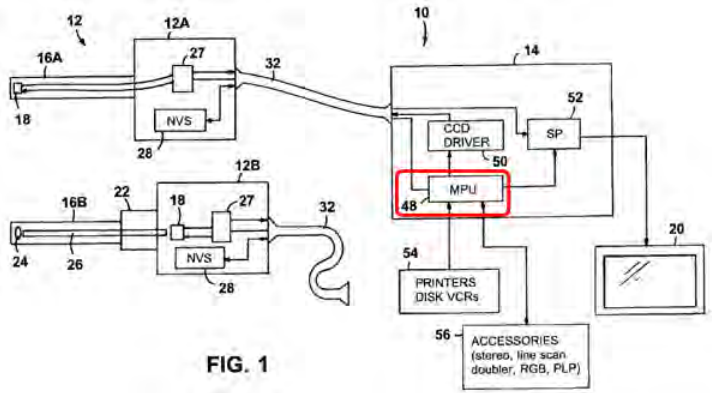
Claims	**Asaida 782**	**in combination with one or more of the following references**
		provides control to CCD driver 50 for transmitting driving signals to CCD 18 in camera head 12. In response to the driving signals, CCD 18 produces electrical signals representing an image of objects within the field of view of CCD 18, and transmits the electrical signals to signal processing circuitry 52. Signal processing circuitry 52 processes the electrical signals from CCD 18 and converts them to video signals for displaying the image on video monitor 20." (Dowdy 082 at 4:60-5:3.)  FIG. 1 Dowdy 082 (Figure 1) "Referring also to FIG. 3, MPU 48 uses the information stored in NVS 28 to control the operation of CCD driver 50 and signal processing circuitry 52. When the user connects cable 32 of camera head 12 to camera processor 14, and, if necessary, powers up video endoscopy system 10, MPU 48 detects the connection and responds by downloading the

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		information from NVS 28 into a memory 58, such as a RAM, of MPU 48 (step 200). MPU 48 reads the stored information out of NVS 28 through a serial data link in cable 32 that includes a CLOCK line 60 controlled by MPU 48 and a DATA line 62 that is shared by NVS 28 and MPU 48." (Dowdy 082 at 5:9-19.) "MPU 48 communicates with signal processing circuitry 52 through a bidirectional serial data link that includes a CLOCK line 80 controlled by MPU 48 and a DATA line 82 that is shared by MPU 48 and signal processing circuitry 52. MPU 48 also controls an ENABLE line 84 that activates external control of signal processing circuitry 52." (Dowdy 082 at 6:1-6.) "After modifying the values of table entries 72-78 received from signal processing circuitry 52, MPU 48 transmits the updated values to signal processing circuitry 52 (step 218). When entries from NVS 28 reflect replacement values for entries in lookup table 68, MPU 48 transmits the replacement values (step 218) without requesting values from signal processing circuitry and modifying those values (steps 208-216)." (Dowdy 082 at 6:18-25.) "After signal processing circuitry 52 receives the updated values from MPU 48 (step 220), signal processing circuitry 52 uses the updated values in processing the electrical signals from CCD 18 for display on video monitor 20 (step 222). That is, signal processing circuitry 52 uses the updated values in locations 69—rather than the nominal values from

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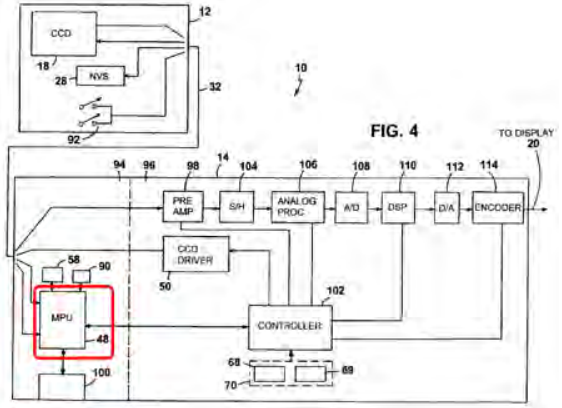
Claims	**Asaida 782**	**in combination with one or more of the following references**
		lookup table 68—in performing the conversion of the electrical signals from CCD 18 to video signals." (Dowdy 082 at 6:26-33.) "Referring to FIG. 4, in a more detailed view, camera head 12 includes CCD 18 (located, as discussed, either in the head or at the tip of the endoscope), NVS 28 and a set of button switches 92 for system control, and camera processor 14 includes a camera controller 94 and a signal processor 96. Cable 32, which connects camera head 12 to camera processor 14, carries drive signals from CCD driver 50 in signal processor 96, electrical signals from CCD 18 to a preamplifier 98 in signal processor 96, data between NVS 28 and MPU 48 in camera controller 94, and signals from button switches 92 to MPU 48." (Dowdy 082 at 6:48-58.)  Dowdy 082 (Figure 4)

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		"MPU 48 controls signal processor 96 in response to signals from button switches 92 and signals from controls in a front panel 100 of camera controller 94. The controls in front panel 100 allow the user of video endoscopy system 10 to configure button switches 92 to perform desired functions. Thus, for example, button switches 92 could be configured to cause signal processor 96 to pause the video image displayed at video monitor 20 (FIG. 1). MPU 48 also displays system parameters at front panel 100, interacts with NVS 28 by downloading information about camera head 12 and updating run time information in NVS 28, updates signal processing parameters in light of the information about camera head 12, and communicates with signal processor 96, all as discussed above." (Dowdy at 6:59-7:5.) Although MPU 48 is located in camera processor 14, it is contained within camera controller 94 which is independent of camera processor 96. Because camera controller 94 and camera processor 96 are independent units housed within camera processor 14, camera controller 94 (and as a result, MPU 48) could have been located in camera head 12. Locating camera controller 94 in the camera head 12 would have been a design option attractive to one of ordinary skill in the art looking to minimize communication circuitry between NVS 28 and MPU 48, as both would be housed within camera 12. "A regulator 19, a programmable nonvolatile memory 20, a CPU 21, a selector (SEL) 22, a supply voltage detector 23, a

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		scope switch 24, and a connector 25 are arranged behind the rear end of the insertion unit 11 of the endoscope 2. The regulator 19 converts a CCD driving voltage fed from a CCD driving power supply 18 incorporated in the image processing apparatus 3A into a desired voltage. The programmable nonvolatile memory 20 in which the endoscope-related data is stored is realized with an EEPROM, a flash ROM, an FRAM, or an MRAM." (Oshima 212 at 6:54-63.) "The CPU 21 includes a one-chip microcomputer for performing a plurality of arithmetic operations including communication and writing, or reading. Specifically, the CPU 21 transmits or receives the endoscope-related data to or from the image processing apparatus 3A through a serial interface, and writes or reads the endoscope-related data in or from the nonvolatile memory 20. The CPU 21 includes a ROM, a RAM, a watchdog timer (WDT), a serial controller (S10), a parallel controller (P10), and a counter (CTC). The selector 22 acts as a serial interface means for transmitting or receiving the endoscope-related data over a sole signal line 49. The supply voltage detector 23 detects a fluctuation or drop in supply voltage and outputs a reset signal, thus preventing a malfunction of the CPU 21 or the nonvolatile memory 20." (Oshima 212 at 6:63-7:10.)

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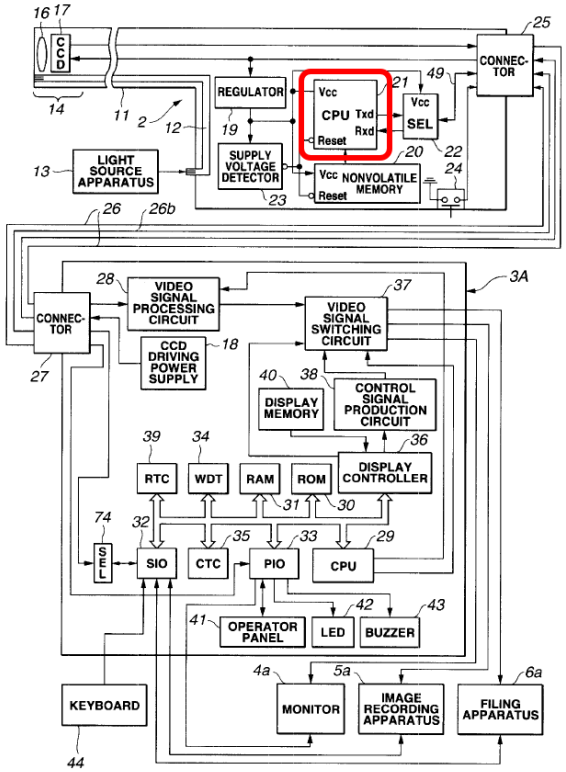
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Oshima 212 (Figure 2)
a memory device, accessible by said processor,	Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005)	"In FIG. 1 and FIG. 2, the circuit configuration of an electronic endoscope according to the embodiment is shown. In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having a number of scanning lines or the like suitable for the scanning line of the

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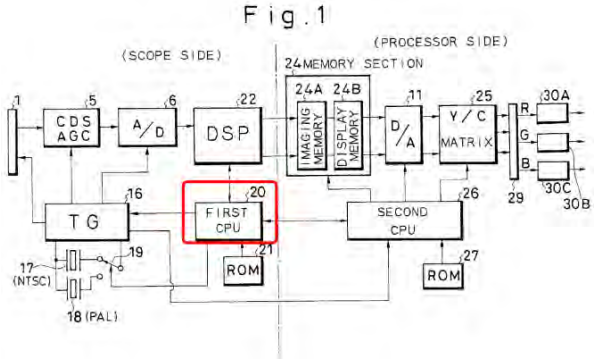
Claims	**Asaida 782**	**in combination with one or more of the following references**
containing camera head information.	(citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)). Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	NTSC system, and to this CCD 1, a timing generator 16 is connected, and to this timing generator 16, an NTSC crystal oscillator 17, a PAL crystal oscillator 18, and a switching device 19 are provided. Furthermore, a first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU 20, either of the oscillators 17, 18 is selected." (Okada 852 at 4:4-15.)  Okada 852 (Figure 1) "A digital section 30 includes a CCD timing generator 32, a static RAM memory 34, a line store timing generator 36, a microprocessor 38, and a USB device interface 40." (Endsley 613 at 3:38-40.) "The output of the line store memory 34 is connected to the host computer 12 via the USB device interface 40, which operates at a maximum data rate of 12 M bits/sec. (See the

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		article 'Universal Serial Bus to Simplify PC I/O', by Michael Slater in *Microprocessor Report*, Volume 9, Number 5, Apr. 17, 1995 for more detail about the benefits of the USB interface.) The microprocessor 38, which may be the Intel 82930 microprocessor, reads data from the line store 34, and transfers the data to the computer 12 via the USB interface 40 (which may be incorporated as part of the microprocessor 38)." (Endsley 613 at 3:51-62.) ***Alternatively***, this limitation is met by camera registers 72. "The operational modes of the camera 10 can be adjusted from the host computer 12. More particularly, the microprocessor 38 includes camera registers 72 that store at least two different camera configurations communicated from the host computer 12 for controlling the image sensor in at least two modes, wherein each configuration includes information defining a plurality of camera parameters as shown in the first column of Table 1." (Endsley 613 at 5:3-10.)

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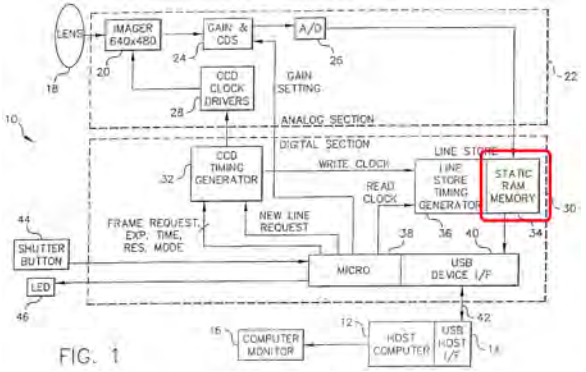
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 FIG. 1 Endsley 613 (Figure 1) ***Alternatively***, this limitation is met by memory in the USB device interface that contains information related to USB descriptors. "The USB interface 40 . . . may be incorporated as part of the microprocessor 38, such as the Intel 82930 microprocessor." (Endsley 613 at 3:43-45.) "USB devices report their attributes using descriptors. A descriptor is a data structure with a defined format. Each descriptor begins with a byte-wide field that contains the total number of bytes in the descriptor followed by a byte-wide field that identifies the descriptor type. "Using descriptors allows concise storage of the attributes of individual configurations because each configuration may reuse descriptors or portions of descriptors from other configurations that have the same characteristics. In this

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		manner, the descriptors resemble individual data records in a relational database." (USB Spec. Rev. 1.0 at 181.) "A device descriptor describes general information about a USB device. It includes information that applies globally to the device and all of the device's configurations. A USB device has only one device descriptor." (USB Spec. Rev. 1.0 at 182.) "A digital section 30 includes a CCD timing generator 32, a static RAM line store memory 34, a line store timing generator 36, a microprocessor 38, and a USB device interface 40." (Endsley 471 at 3:19-22.) "The output of the line store memory 34 is connected to the host computer 12 via the USB device interface 40, which operates at a maximum data rate of 12M bits/sec. (See the article 'Universal Serial Bus to Simplify PC I/O', by Michael Slater in Microprocessor Report, Volume 9, Number 5, Apr. 17, 1995 for more detail about the benefits of the USB interface.) The USB interface 40, which may be incorporated as part of the microprocessor 38, such as the Intel 82930 microprocessor, reads data from the line store 34." (Endsley 471 at 3:37-46.) "[T]he present invention includes a novel way of 'line throttle clocking' the image sensor 20 by varying a line blanking interval 68 from line to line, as shown in FIG. 5, so as to transfer lines of data from the CCD image sensor 20 into the line store memory 34 at the appropriate time." (Endsley 471

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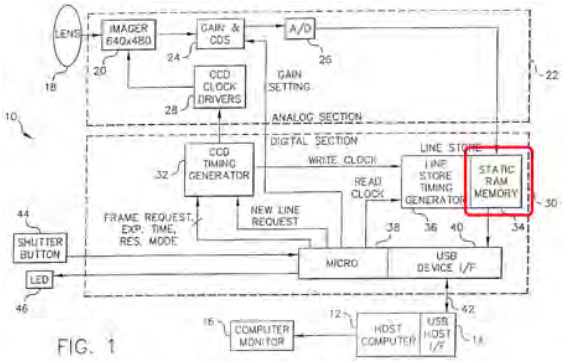
Claims	**Asaida 782**	**in combination with one or more of the following references**
		at 4:54-59.) "FIG.5 shows that, once the image data is transferred by the readout pulse 60 to the light-protected vertical registers 50, the line clocking is 'throttled' to accommodate the storage capacity of the line store memory 34. The line store memory 34 is capable of storing a small number of lines of data and provides block transfer capability at low cost. Whenever the line store memory 34 has sufficient room to accommodate a new line of image data, the timing generator 32 creates the vertical and horizontal timing pulses 62 and 64 needed to read out the next line from the image sensor, as shown in FIG. 5, and then returns to a wait state until sufficient data is transferred from the line store memory 34 to the computer 12 so as to provide room for the next line. Since the waiting period (equal to the line blanking time) depends on the USB bus traffic, the line readout times and frame readout times are variable, rather than fixed, as in prior art cameras." (Endsley 471 at 4:60-5:9.)  FIG. 1

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		Endsley 471 (Figure 1) ***Alternatively***, this limitation is met by memory in the USB device interface that contains information related to USB descriptors. "The USB interface 40 . . . may be incorporated as part of the microprocessor 38, such as the Intel 82930 microprocessor." (Endsley 471 at 3:43-45.) "USB devices report their attributes using descriptors. A descriptor is a data structure with a defined format. Each descriptor begins with a byte-wide field that contains the total number of bytes in the descriptor followed by a byte-wide field that identifies the descriptor type. "Using descriptors allows concise storage of the attributes of individual configurations because each configuration may reuse descriptors or portions of descriptors from other configurations that have the same characteristics. In this manner, the descriptors resemble individual data records in a relational database." (USB Spec. Rev. 1.0 at 181.) "A device descriptor describes general information about a USB device. It includes information that applies globally to the device and all of the device's configurations. A USB device has only one device descriptor." (USB Spec. Rev. 1.0 at 182.) "An apparatus sends electrical signals that represent an

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		optical image to a processor for conversion to video signals suitable for display on a display device. The apparatus includes a device for insertion into a region to be viewed for developing an optical image of the region, an imager for generating electrical signals that represent the optical image, and a digital memory for storing information about the imager. The device is adapted to be connected to the processor so that the processor can receive the electrical signals from the imager and obtain information from the digital memory. The processor uses the information from the digital memory in performing the conversion." (Dowdy 082 at Abstract.) "The camera head and endoscope are typically detachable as a unit from the control unit so that a variety of camera heads can be used with a single control unit. This offers a number of advantages. For example, if a first camera head fails, the control unit can be operated with another camera head while the first camera head is being serviced. Also, different types of camera heads, each of which may be most useful for certain procedures, can be used with a single control unit so as to avoid the expense of purchasing and maintaining multiple control units." (Dowdy 082 at 1:25-34 (Background of the Invention).) "In one general aspect, this invention features an apparatus for providing electrical signals that represent an optical image to a processor for conversion to video signals suitable for display on a display device. The apparatus includes a device for insertion into a region to be viewed for developing

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		an optical image of the region, an imager for generating electrical signals that represent the optical image, and a digital memory for storing information about the imager. The device is adapted to be connected to the processor so that the processor can receive the electrical signals from the imager and obtain information from the digital memory. The processor uses the information from the digital memory in performing the conversion." (Dowdy 082 at 1:38-50 (Summary of the Invention).) "The digital memory stores information about the configuration of the imager. This information can include the location of the imager relative to the device. For example, the information identifies whether the imager is located at the distal end or the proximal end of the device. The imager is a charge coupled device. The information identifies an optical format size of the charge coupled device." (Dowdy 082 at 1:53-59.) "The digital memory also stores information about variations in performance characteristics of the imager relative to nominal performance characteristics. When the apparatus includes optics, the information in the digital memory accounts for variations in performance characteristics of the optics relative to nominal performance characteristics. Similarly, when the imager includes a charge coupled device or a cable for connection to the processor, the information accounts for variations in performance characteristics of the charge coupled device or the cable relative to nominal performance characteristics. The information also identifies

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		variations in luminance and color reproduction by the imager." (Dowdy 082 at 1:60-2:5 (Summary of the Invention).) "When the apparatus is designed for application to particular regions, the information identifies characteristics of the region to be viewed by the imager. This allows the processor to optimize the conversion for parameters that are desirable in a particular application." (Dowdy 082 at 2:6-10.) "In one embodiment, the digital memory is a non-volatile storage device, and can be implemented using an EEPROM." (Dowdy 082 at 2:16-17.) "When the information stored in the digital memory identifies the configuration of the device, the processor modifies the conversion based on the configuration. This allows the processor to automatically optimize the conversion for different configurations of the device." (Dowdy 082 at 2:34-38.) "Referring also to FIG. 2, to enable different types of camera heads 12 to be used with camera processor 14 without impacting the quality of the video image displayed on video monitor 20, each camera head 12A, 12B (referred to generally with reference numeral 12) includes a non-volatile storage device ("NVS") 28 that stores information identifying the configuration 30 of the particular camera head 12A, 12B. Camera processor 14 uses the information stored in NVS 28 to modify processing of the electrical

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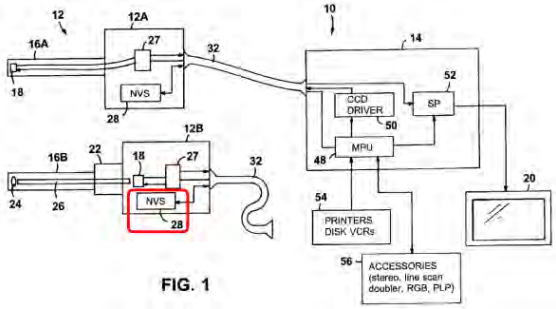
Claims	**Asaida 782**	**in combination with one or more of the following references**
		signals produced by camera head 12, and thereby accounts for the properties of the configuration 30 to which camera head 12 belongs. In a preferred embodiment, NVS 28 is implemented as an electrically erasable programmable read only memory ("EEPROM"). One such EEPROM is an eight pin, 256 byte storage capacity memory available from the Xicor Corp. as model number 24XC02." (Dowdy 082 at 3:62-4:10.)  FIG. 1 Dowdy 082 (Figure 1)

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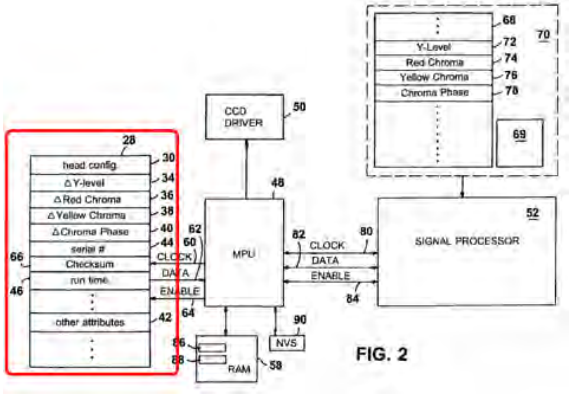
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 FIG. 2 Dowdy 082 (Figure 2) "In addition to variations caused by the configuration of camera head 12, the electrical signals produced by camera head 12 can also vary, because performance characteristics of camera heads 12 tend to vary from device to device. These variations, which are caused primarily by differences in optics, CCDs 18, and cables 32 that are attached to camera heads 12 and connect camera heads 12 to camera processor 14, can adversely affect the ability of a camera head 12 to produce electrical signals that result in an optimal video image. Thus, to further ensure consistent performance when different camera heads 12 are used, NVS 28 also stores information that identifies variations in the performance characteristics of a particular camera head 12 from nominal values." (Dowdy 082 at 4:11-24.) "To enable the video image produced at video monitor 20 to

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		be optimized for certain procedures, the NVS 28 of a camera head 12 designed for those procedures can include information 42 that is used by camera processor 14 to optimize certain signal processing attributes. For example, in a camera head 12 designed for procedures requiring improved edge definition, NVS 28 stores edge enhancement information 42 that replaces nominal edge enhancement values stored within and used by camera processor 14. Similarly, in camera heads 12 designed for procedures in which the white or grey brightness ranges are of particular interest, NVS 28 stores information 42 that modifies, respectively, operation of the so-called "knee circuit" (which implements a nonlinear function for compressing, rather than clipping, the upper level, white, component of the video signal) and the operation of the so-called "gamma circuit" (which implements a nonlinear function for optimizing the median level, grey, component of the video signal) implemented by signal processor 14." (Dowdy 082 at 4:36-54.) "For servicing and other purposes, NVS 28 also stores information that identifies the serial number 44 of camera head 12 and a measure 46, in minutes and hours, of the run time that camera head 12 has experienced." (Dowdy 082 at 4:55-58.) "Referring also to FIG. 3, MPU 48 uses the information stored in NVS 28 to control the operation of CCD driver 50 and signal processing circuitry 52. When the user connects cable 32 of camera head 12 to camera processor 14, and, if

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		necessary, powers up video endoscopy system 10, MPU 48 detects the connection and responds by downloading the information from NVS 28 into a memory 58, such as a RAM, of MPU 48 (step 200). MPU 48 reads the stored information out of NVS 28 through a serial data link in cable 32 that includes a CLOCK line 60 controlled by MPU 48 and a DATA line 62 that is shared by NVS 28 and MPU 48." (Dowdy 082 at 5:9-19.) "Referring to FIG. 4, in a more detailed view, camera head 12 includes CCD 18 (located, as discussed, either in the head or at the tip of the endoscope), NVS 28 and a set of button switches 92 for system control, and camera processor 14 includes a camera controller 94 and a signal processor 96. Cable 32, which connects camera head 12 to camera processor 14, carries drive signals from CCD driver 50 in signal processor 96, electrical signals from CCD 18 to a preamplifier 98 in signal processor 96, data between NVS 28 and MPU 48 in camera controller 94, and signals from button switches 92 to MPU 48." (Dowdy 082 at 6:48-58.)

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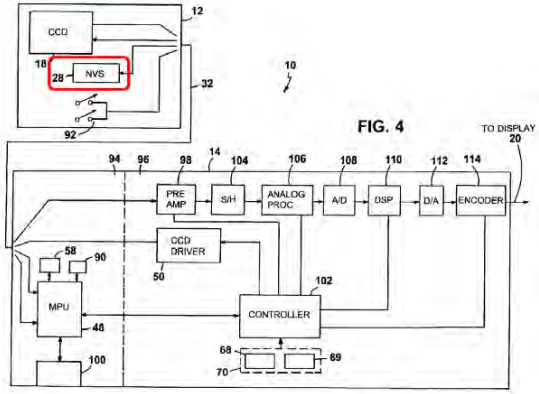
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Dowdy 082 (Figure 4) "MPU 48 controls signal processor 96 in response to signals from button switches 92 and signals from controls in a front panel 100 of camera controller 94. The controls in front panel 100 allow the user of video endoscopy system 10 to configure button switches 92 to perform desired functions. Thus, for example, button switches 92 could be configured to cause signal processor 96 to pause the video image displayed at video monitor 20 (FIG. 1). MPU 48 also displays system parameters at front panel 100, interacts with NVS 28 by downloading information about camera head 12 and updating run time information in NVS 28, updates signal processing parameters in light of the information about camera head 12, and communicates with signal processor 96, all as discussed above." (Dowdy at 6:59-7:5.) "A nonvolatile, programmable memory is incorporated in an

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		endoscope. Endoscope-related data closely relevant to the endoscope, such as, an endoscope model name and the number of power feeds are stored in the nonvolatile memory. The endoscope is connected to an external image processing apparatus, and endoscope-related data is read from the nonvolatile memory. Based on the read endoscope-related data, the use situation of the endoscope is grasped or the endoscope is managed. The number of power feeds is varied depending on the use situation of the endoscope, and written in the nonvolatile memory. Thus, the endoscope-related data is used to maintain the endoscope and reduce a load to be incurred by the external image processing apparatus that is a connected apparatus. Consequently, the endoscope can be managed and maintained easily using a small software system." (Oshima 212 at Abstract.) "[An] object of the present invention is to provide an endoscope system in which endoscope-related data including a use situation of an endoscope can be checked readily." (Oshima 212 at 1:60-62.) "A regulator 19, a programmable nonvolatile memory 20, a CPU 21, a selector (SEL) 22, a supply voltage detector 23, a scope switch 24, and a connector 25 are arranged behind the rear end of the insertion unit 11 of the endoscope 2. The regulator 19 converts a CCD driving voltage fed from a CCD driving power supply 18 incorporated in the image processing apparatus 3A into a desired voltage. The programmable nonvolatile memory 20 in which the endoscope-related data is stored is realized with an

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		EEPROM, a flash ROM, an FRAM, or an MRAM." (Oshima 212 at 6:54-63.) "Especially important data out of endoscope-related data storable in the nonvolatile memory 20 includes, for example, an endoscope model name, the structure of the distal part of an endoscope, a cleaning tube/adaptor name, a CCD model name, a type of optical filter in a CCD, information relating to the channels in an endoscope, information relating to the switches on an endoscope, a version number, and identification data." (Oshima 212 at 29:16-25.)

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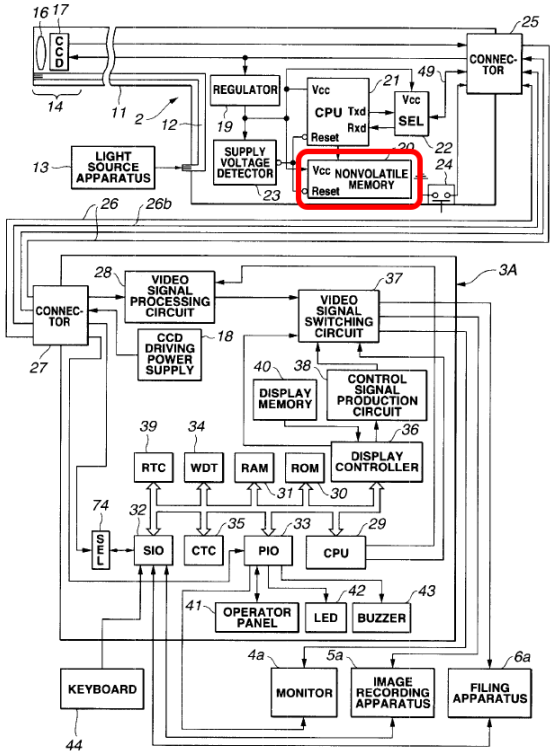
Claims	**Asaida 782**	**in combination with one or more of the following references**
		 Oshima 212 (Figure 2) "FIG. 35 describes processing to be performed in the image processing apparatus 3A, which has the ability to communicate with the endoscope 2 and is connected to the endoscope 2, for treating count data contained in data to be stored in the nonvolatile memory 20 in the endoscope 2." (Oshima 212 at 29:59-63.)

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		"The connected apparatus 3A uses connection sensing means (not shown) incorporated in the endoscope and the connected apparatus to judge whether it has been connected to the endoscope 2 (S321). If connection is sensed, identification data or an endoscope model name is read first (S322)." (Oshima 212 at 29:66-30:4.) "From the foregoing description of the prior art, it is clear that the 'bad pixel' data is never transferred to the camera portion, but instead remains in the local controller memory. Accordingly if a camera has been subjected to pixel evaluation for existence of blemishes using a CCU with a blemish compensating capacity as described above, another camera cannot be used in its place with the same CCU unless the CCU blemish compensator is again operated to evaluate the pixels of the new camera. Moreover, assuming that blemish compensation is desired, a camera that has been evaluated by the CCU of Fig. 1 is not interchangeable with another like blemish compensator-equipped CCU unless it is first re-evaluated for blemishes." (Zu 391 at 5-6.) "This non-interchangeability of cameras with a CCU is especially limiting in the case of video endoscopes. During surgery, it may be necessary to employ two or more video endoscopes when only one CCU may be available. With a compensator-equipped CCU as shown in Fig. 1, substitution of one video camera endoscope for another may be frustrated by the need to first evaluate the camera for blemishes and record the 'bad pixels' in the CCU's digital memory so that

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		compensation may be accomplished when video information is acquired by the endoscope's camera." (Zu 391 at 6.) "The object of this invention is to facilitate use of video cameras having known pixel blemishes with different camera control units." (Zu 391 at 6.) "The present invention comprises incorporating into a CCD-type video camera an electronically programmable non-volatile memory which stores the location of 'bad' pixels and is controlled by a device which is located remotely from the camera in a separate CCU. This arrangement assures that video cameras are interchangeable with CCU's regardless of CCD blemish content." (Zu 391 at 6.) "Fig. 2 illustrates the invention. Except as described hereinafter, the system shown in Fig. 2 incorporates the same elements and the same functions as the system of Fig. 1, and identical elements are identified by the same numerals. In this case, the camera 2 is modified by incorporating therein an electronically programmable non-volatile digital memory 42 which is coupled to camera connector 14 via a suitable bus 44." (Zu 391 at 7.)

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		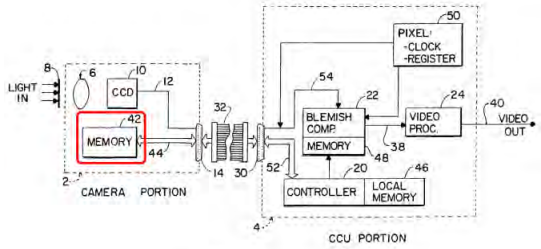 FIG. 2 Zu 391 (Figure 2) "In the operational mode, the data in memory 42 is transferred to memories 46 and 48 whenever the unit is energized. The blemish compensation operation is then performed by the blemish compensator 22 using pixel address data downloaded from camera memory 42. The pixel address data is downloaded from camera memory 42 to blemish compensator memory 48 by the controller 20 via the buses 44 and 52." (Zu 391 at 8.) "When the operational mode is initiated with the camera coupled to a CCU 4 as described, the controller 22 downloads the pixel address data from the camera's memory 42 to the protected local memory 46 of the controller 20. Subsequently that data is loaded into the volatile memory 48 of the blemish compensator 22. Typically this data transfer from camera memory 42 t the local memory 46 of the controller occurs after a forced rest imposed by controller 20, which clears, resets, and reloads all non-protected CCU memory." (Zu 391 at 9.)

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22. The video imaging system according to claim 21 wherein said camera head further comprises a multiplexer, for generating a multiplexed signal, which includes the image signal and control signals.	*See* Claim 21. The analysis of Claim 21 is incorporated by reference in its entirety. "The multiplexor 18 is supplied with control data D_{CTL} from a synchronizing circuit block 19 and a control circuit block 20, while being supplied with voice data D_{MIC}, from a microphone signal inputted from a microphone input terminal 21 by means of a selector 22 and digitized by an A/D converter 23 into audio data $D_{MIC/AUDIO}$. The multiplexor 18 adds the signals D_{CTL} and $D_{MIC/AUDIO}$ to a digital video signal D_{VIDEO} composed of the digital component Video signals D_Y, D_{CR} and D_{CB} or the digital composite video signal D_{CS} supplied from the encoder 14. Output data D_{MPX} from the multiplexor 18, that is, the digital video signal D_{VIDEO} added to the control data D_{CTL} and the audio data $D_{MIC/AUDIO}$, are outputted in parallel at a parallel output port 24, while being converted by P/S converter 25 from parallel data into serial data which are serially outputted at a serial output port 26." (Asaida 782 at 6:67-7:15.)	"As generally used, the USB interface has a clock rate of 12 MHz. The clock is transmitted encoded along with the differential data, and the data is transferred in packets. A SYNC field precedes each data packet to allow the receiver(s) to synchronize their bit recovery clocks. The basic unit scheduling is 1 mSec. All bus transactions involve the transmission of up to three packets, which include from 1 to 1024 bytes of data plus a 3 bytes header that includes an error detection code word." (Endsley 613 at 3:66-4:7.) Thus, the clock cycle is multiplexed with the differential data and transferred in packets.

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	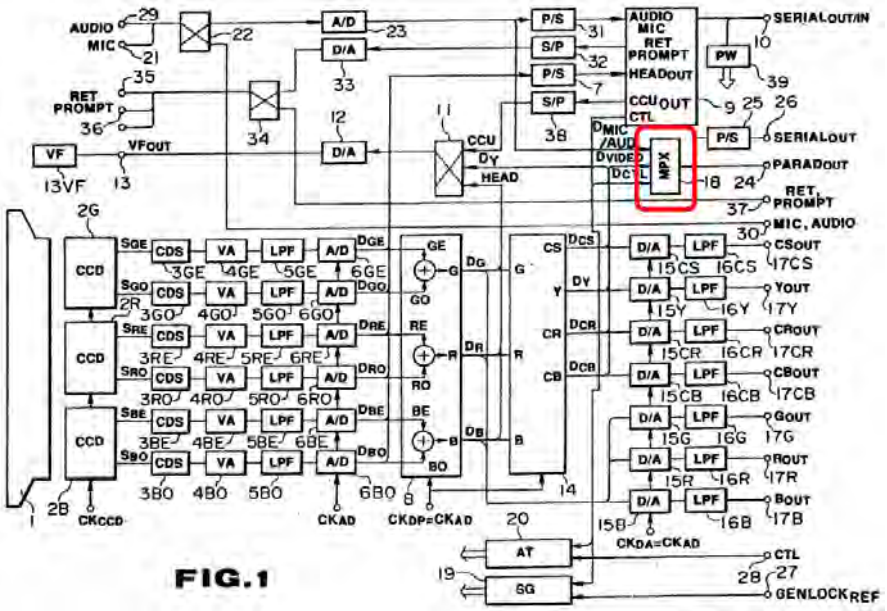 Asaida 782 (Figure 1)	
25. The video imaging system according to claim 21 wherein said camera head utilizes at least one	*See* Claim 21. The analysis of Claim 21 is incorporated by reference in its entirety. Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005) (citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)).	"Reference is now made to FIG. 4, which is an schematic block diagram of the miniature endoscope according to a preferred embodiment of the present invention. Parts that are identical to those shown above are given the same reference numerals and are not referred to again except as necessary for an understanding of the present embodiment. Optical assembly 48 receives light, indicated by arrows 60, from an object being viewed. The light is processed by optical assembly 48, as will be explained below, to reach image sensor 46 were it is converted from photons into electrical

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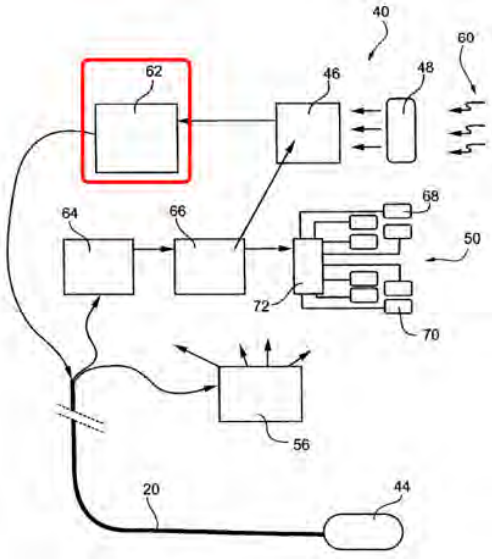
Claims	**Asaida 782**	**in combination with one or more of the following references**
digital serial driver utilizing Low-Voltage Differential Signals.	Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	signals. The electrical signals are digitized and passed to a transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Adler 940 at 10:7-19.)  Adler 940 (Figure 4) "Figure 1 shows a typical connection with LVDS drivers and receivers."

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		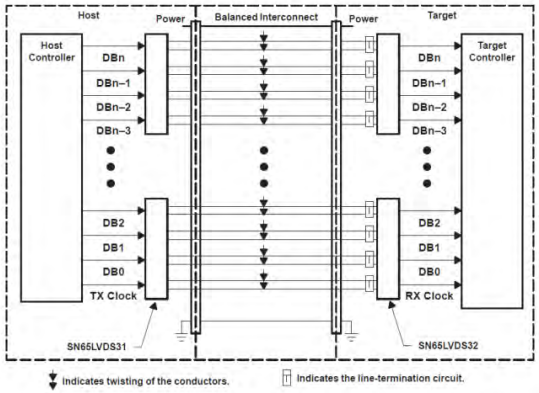 Figure 1. Typical Connection With LVDS Drivers and Receivers TI LVDS (Figure 1) "The LVDS driver produces a differential voltage across a 100-Ω load in the range of 247 mV to 454 mV with a typical offset voltage of 1.2 V relative to ground (see Figure 2). Most drivers are commonly imple3mented as current-mode devices, which allow frequency to be virtually independent of power consumption. These two characteristics, low voltage swings and constant current, allow LVDS drivers to operate at higher data rates and lower power dissipation." (TI LVDS at 2.) "As the need for higher bandwidth accelerates, system designers are choosing differential signaling to satisfy high bandwidth requirements while reducing power, increasing noise immunity, and decreasing EMI emissions. LVDS is a low swing, differential signaling technology providing very

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		fast data transmission, common-mode noise rejection, and low power consumption over a broad frequency range. The Virtex-E family delivers the programmable industry's highest bandwidth and most flexible differential signaling solution for direct interfacing to industry-standard LVDS devices." (Virtex-E LVDS at 1.) "With up to 36 I/O pairs operating at 622 Megabits per second (Mb/s) or up to 344 I/O pairs operating at over 311 Mb/s, the Virtex-E family supports multiple 10 Gb/s ports while maintaining high signal integrity with low power consumption. Unlike other PLD solutions, all Virtex-E LVDS I/Os support input, output, and I/O signaling, providing a system designer unparalleled flexibility in board layout." (Virtex-E LVDS at 1.) Advantages of LVDS include: "• LVDS is specified to be technology and process independent. • LVDS is EMI tolerant. Common-mode noise is equally removed by two conductors and rejected by the receiver. • No transmission medium is defined in the standard. The medium can be tailored to meet the specific application requirements. • The typical LVDS voltage swing is 350 mV, resulting in a higher transfer rate and lower power consumption." (Virtex-E LVDS at 2.) "There are two configurations that are used in LVDS applications, point-to-point and multi-drop. The Virtex-E

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Claims	**Asaida 782**	**in combination with one or more of the following references**
		family supports both LVDS configurations. **Point-to-Point** In point-to-point configuration, there is one transmitter and one receiver. The LVDS driver is a current source that drives a differential pair of lines. The typical current drive is 3.5 mA. The receiver has high DC impedance. The majority of the driver current flows across the termination resistor generating about 350 mV at the receiver inputs (Figure 1). **Multi-Drop** A multi-drop LVDS configuration has one transmitter and multiple receivers. The differential termination resistor is placed close to the last receiver (Figure 3)." (Virtex-E LVDS at 2.) Among the many applications that LVDS is suited for are "digital cameras" and "multimedia peripherals." (Virtex-E LVDS at 2-3.) "Figure 1 shows the schematic of a standard LVDS driver driving the Virtex-E receiver. An LVDS driver drives the two 50 W transmission lines into a Virtex-E LVDS receiver. The two 50 W single-ended transmission lines can be micro-strip, strip-line, a 100 W differential twisted pair, or a similar balanced differential transmission line." (Virtex-E LVDS at 3.)

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		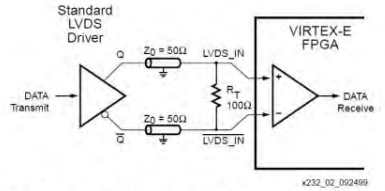 **Figure 1: A Standard LVDS Driver Driving a Virtex-E LVDS Receiver** Virtex-E LVDS (Figure 1) "As may be seen, the circuit of FIG. 4 employs a plurality of LVDS circuits 11. Each circuit 11 includes a respective driver 54 and a respective receiver 56. Each driver 54 receives a respective input signal Din0, Din1 . . . Dinn, which are digital logic levels of, for example, 3.3 volts for logic "1" and zero volts for logic "0". Changes in state in these signals are transmitted over the differential lines to the respective receivers 56. Each receiver 56 generates a respective output signal Dout0, Dout1, . . . Doutn, which are at the several hundred millivolt level." (Chung 290 at 2:27-36.)

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		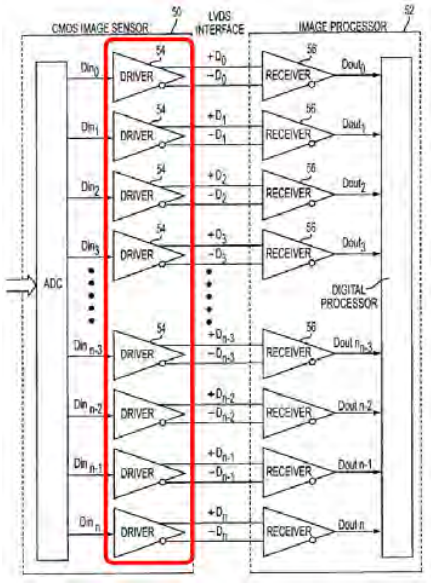 Chung 290 (Figure 4)
26. The video imaging system according to claim 21 wherein said camera control unit utilizes at least one	*See* Claim 21. The analysis of claim 21 is incorporated by reference in its entirety. Even if a piece of prior art does not expressly disclose a particular limitation of the asserted claim, it anticipates if a person of ordinary skill in the art could combine the prior art description with his or her own knowledge to make the claimed invention. *See Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005) (citing *Helifix Ltd. v. Blok-Lok., Ltd.*, 208 F.3d 1339, 1347 (Fed. Cir. 2000)).	"Reference is now made to FIG. 4, which is an schematic block diagram of the miniature endoscope according to a preferred embodiment of the present invention. Parts that are identical to those shown above are given the same reference numerals and are not referred to again except as necessary for an understanding of the present embodiment. Optical assembly 48 receives light, indicated by arrows 60, from an object being viewed. The light is processed by optical assembly 48, as will be explained below, to reach image sensor 46 were it is converted from photons into electrical signals. The electrical signals are digitized and passed to a

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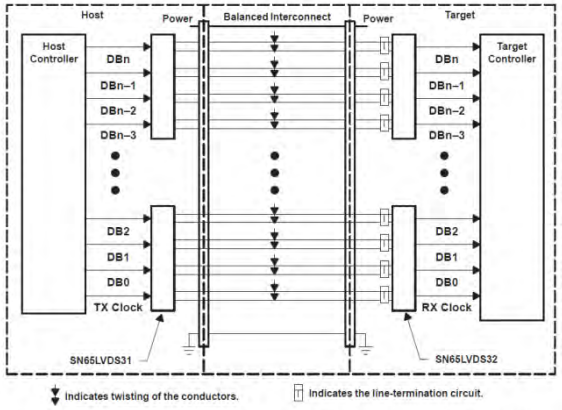
digital serial receiver utilizing Low-Voltage Differential Signals.	Accordingly, even if Asaida 782 does not expressly or inherently disclose this claim element, the claim would have been an obvious design choice based on the inherent disclosure of the references and/or the knowledge of one of ordinary skill in the art at the time of the alleged invention of the '310 patent.	transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Adler 940 at 10:7-19.) If the electrical signals are transmitted to the processing device 30 using an LVDS transmitter, the at least one digital serial receiver in the processing device that receives the signals must necessarily utilize Low-Voltage Differential Signals. "Figure 1 shows a typical connection with LVDS drivers and receivers."  Figure 1. Typical Connection With LVDS Drivers and Receivers TI LVDS (Figure 1) "The recommended voltage applied to the receiver is

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		between ground and 2.4 V with a common mode range of 0.2 V to 2.2 V. The receiver has a sensitivity level of ±100 mV to correctly assume the intended binary state (see Figure 2). The LVDS interconnecting media must be matched with the 100-Ω termination resistor located at the inputs of the receiver." (TI LVDS at 4.) "There are two configurations that are used in LVDS applications, point-to-point and multi-drop. The Virtex-E family supports both LVDS configurations. **Point-to-Point** In point-to-point configuration, there is one transmitter and one receiver. The LVDS driver is a current source that drives a differential pair of lines. The typical current drive is 3.5 mA. The receiver has high DC impedance. The majority of the driver current flows across the termination resistor generating about 350 mV at the receiver inputs (Figure 1). **Multi-Drop** A multi-drop LVDS configuration has one transmitter and multiple receivers. The differential termination resistor is placed close to the last receiver (Figure 3)." (Virtex-E LVDS at 2.) Among the many applications that LVDS is suited for are "digital cameras" and "multimedia peripherals." (Virtex-E LVDS at 2-3.) "Figure 1 shows the schematic of a standard LVDS driver

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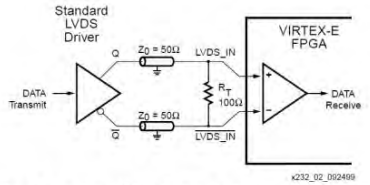
		driving the Virtex-E receiver. An LVDS driver drives the two 50 W transmission lines into a Virtex-E LVDS receiver. The two 50 W single-ended transmission lines can be micro-strip, strip-line, a 100 W differential twisted pair, or a similar balanced differential transmission line." (Virtex-E LVDS at 3.)  Figure 1: A Standard LVDS Driver Driving a Virtex-E LVDS Receiver Virtex-E LVDS (Figure 1) "As may be seen, the circuit of FIG. 4 employs a plurality of LVDS circuits 11. Each circuit 11 includes a respective driver 54 and a respective receiver 56. Each driver 54 receives a respective input signal Din0, Din1 . . . Dinn, which are digital logic levels of, for example, 3.3 volts for logic "1" and zero volts for logic "0". Changes in state in these signals are transmitted over the differential lines to the respective receivers 56. Each receiver 56 generates a respective output signal Dout0, Dout1, . . . Doutn, which are at the several hundred millivolt level." (Chung 290 at 2:27-36.)

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		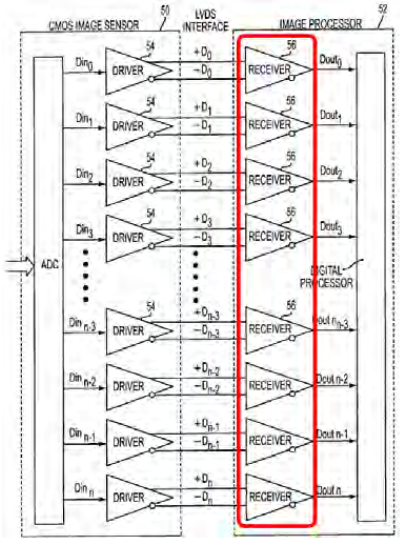 Chung 290 (Figure 4)